OZ9906

White LED Backlight Controller

FEATURES

- Switch-mode DC/DC controller to balance LED current
- High current output drive for 6 LED strings
- Spread spectrum feature on operating frequency
- High efficiency LED current regulation
- Supports analog and external PWM dimming
- User-defined phase shift PWM dimming function with 2 to 6 phase options
- PWM dimming frequency synchronization
- MOSFET over-current protection
- LED Short-circuit protection
- User-defined short-circuit protection threshold
- LED fault STATUS output

ORDERING INFORMATION

Order Information	Temp Range	Package
OZ9906GN	-20°C to +85°C Note 3, Page 3	28-pin SOP Lead-Free

GENERAL DESCRIPTION

OZ9906 is a high efficiency switch-mode DC/DC controller that drives up to 6 LED strings connected in parallel. OZ9906 is targeted for large size monitor and TV applications.

OZ9906 provides six (6) LED current sense inputs. The IC provides individual LED current regulation for each LED string. This allows the backlight to remain functioning in the event that any string(s) is damaged during normal operation.

The operation frequency is user-defined with spread spectrum operation feature that minimizes system EMI during operation.

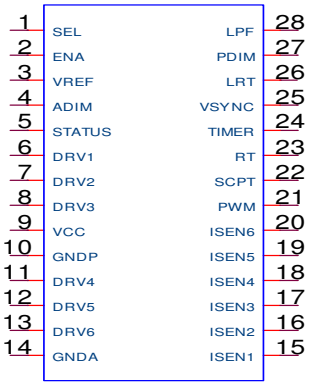
The controller provides an internal phase-shift PWM dimming function, where the PWM dimming signal is phase-shifted by 60 degrees between strings when all 6 strings are connected.

The number of phases is selectable from 2 to 6 phases depending upon the number of strings connected. The proprietary feature reduces output current ripple and improves the quality of the LCD display.

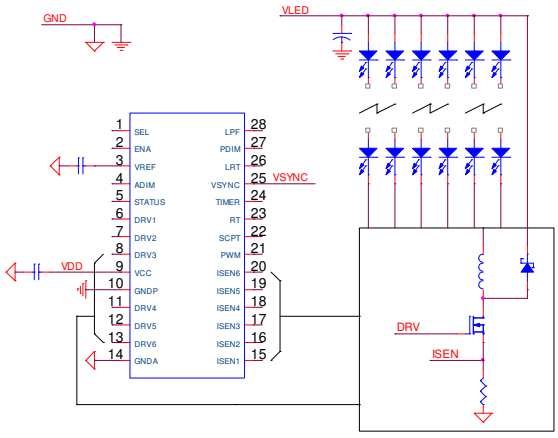
OZ9906 supports external PWM dimming and analog dimming control, providing the most flexible solution for LED display applications. The internal PWM frequency can be synchronized with an external pulse signal.

The IC provides protections including LED over-current, LED short-circuit, Power MOSFET over-current, LED open/short circuit and a fault STATUS output.

PIN DIAGRAM



TYPICAL OPERATING CIRCUIT



PIN DESCRIPTION

Name	Pin No.	I/O[1]	Description
SEL	1	I	Internal PWM Synchronization ratio Selection
ENA	2	I	IC Enable
VREF	3	I/O	Reference Voltage
ADIM	4	I	Analog Dim Input
STATUS	5	O	LED Operation Status (Open Drain) Output
DRV1	6	O	Drive Output for LED Current Regulation- String 1
DRV2	7	O	Drive Output for LED Current Regulation- String 2
DRV3	8	O	Drive Output for LED Current Regulation- String 3
VCC	9	-	Power Supply Input of IC.
GNDP	10	-	Power Ground
DRV4	11	O	Drive Output for LED Current Regulation- String 4
DRV5	12	O	Drive Output for LED Current Regulation- String 5
DRV6	13	O	Drive Output for LED Current Regulation- String 6
GNDA	14	-	Analog Ground
ISEN1	15	I	LED Current Sense for String 1
ISEN2	16	I	LED Current Sense for String 2
ISEN3	17	I	LED Current Sense for String 3
ISEN4	18	I	LED Current Sense for String 4
ISEN5	19	I	LED Current Sense for String 5
ISEN6	20	I	LED Current Sense for String 6
PWM	21	I	External PWM Dim Signal Input
SCPT	22	I	Setting for Short Circuit Protection Threshold
RT	23	I/O	Resistor to Set Operation Frequency
TIMER	24	I/O	Protection Delay Timer
VSYNC	25	I	Internal PWM Synchronization Signal Input
LRT	26	I/O	Resistor to set internal dimming frequency
PDIM	27	I	DC Voltage for Internal PWM Duty Cycle Control
LPF	28	I/O	Low Pass Filter for Internal PWM Synchronization

Note[1]: I= Input, O= Output, I/O= Input/Output

ABSOLUTE MAXIMUM RATINGS[2]

Input Voltage-VCC	-0.3V to 20.0V
GNDA, GNDP	+/- 0.3V
DRV1/2/3/4/5/6	-0.3V to VCC
All Other Pins	-0.3V to VREF + 0.3V
Operating Junction Temperature[3]	150°C
Storage Temperature	-55°C to 150°C

RECOMMENDED OPERATING RANGE

Input Voltage- VCC		7.0V to 16.0V
DRV1/2/3/4/5/6		GNDP to VCC
All Other Pins		GNDA to VREF
Balance Switching Frequency		100kHz – 1.0MHz
Internal PWM Dimming Frequency		2kHz to 10kHz / channel
Operating Temperature Range[3]		-20°C to +85°C
Operating Junction Temperature[3]		≤125°C
Thermal Impedance[3,4]	θ_{J-C}	θ_{J-A}
28-pin SOP	6 °C/W	70 °C/W

Note[2]: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed and may cause permanent damage to the IC. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the Electrical Characteristics section of the specification is not implied. The "Electrical Characteristics" table defines the conditions for actual device operation. Exposure to absolute maximum rated conditions for extended periods may affect device reliability

Note[3]: Not to exceed the maximum junction temperature of the IC, which relates to the operating power of the IC and the thermal resistance of the IC/package as above. For a typical application (refer to the Reference Application Circuit, Figure 4, Page 10), the operation power of the IC can be calculated by $P_D = V_{DD} \times I_{DD}$, where V_{DD} represents the input voltage at pin VCC of the IC and I_{DD} represents the current flow into pin VCC of the IC.

- Using OZ9906 in an application circuit with an ambient temperature near 85°C, the recommended power dissipation of the 28 SOP package is approximately 286mW.
- It is recommended that the customer contact their local O2Micro Field Application Engineer (FAE), if the application is significantly different from the Reference Application Circuit illustrated in Figure 4, Page 10.

Note[4]: Still air, low effective thermal conductivity board per JESD51-3.

ELECTRICAL CHARACTERISTICS[5]

All specifications below are at: T_a=25^{0}C, VCC=12.0V R_{RT}=51.1KΩ, LPF=5.0V, SEL=5V, R_{LRT}= 100.0KΩ unless otherwise noted

PARAMETER	SYMBOL	CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Operating Current			TBD	25	TBD	mA
Standby Current				-	2.0	µA
Enable & Under-Voltage Lockout						
ENA Logic	Enable		2.0	-	-	V
	Disable		-	-	1.0	V
VCC Under-Voltage Lockout Logic	Resume		6.8	-	-	V
	Lockout		-	-	6.5	V
Reference Voltage						
Reference Voltage	VREF	I_{REF}= 1.0mA		5.00		V
		Temperature Coefficient				ppm/ ^{O}C
ISEN Maximum Regulation Threshold	ISEN			500		mV
		Temperature Coefficient	-		-	ppm/℃
ISEN Minimum Regulation Threshold				100		mV
		Temperature Coefficient	-		-	ppm/℃
Driver						
DRV 1 ~ 6 Source Resistance	Ron			15		Ω
DRV 1 ~ 6 Sink Resistance	Ron			8		Ω
Control & Protection						
PWM Duty Cycle Balance Rate		DIM= 1.4V	-	+/-5.0		%
Oscillator						
Operation Frequency	f_{OP}	Measured on DRV pins		430		kHz
		Temperature Coefficient	-		-	ppm/℃
Internal PWM Dimming Frequency	f_{LFOSC}			5.6		kHz
		Temperature Coefficient	-		-	ppm/℃

Note[5]: Use of this product outside the limits of the test conditions may experience in a variation of parameters from the published parameters. If additional information is needed, please consult with your O2Micro Field Application Engineer (FAE).

PARAMETERS GUARANTEED BY DESIGN[6]

PARAMETER	SYMBOL	CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Reference Voltage						
TIMER Charging Current				3		uA
TIMER Protection Threshold				3		V
Driver Logic						
Minimum-On Time for DRV 1~6			TBD	400	TBD	ns

Note[6]: Parameters Guaranteed By Design

FUNCTIONAL BLOCK DIAGRAM

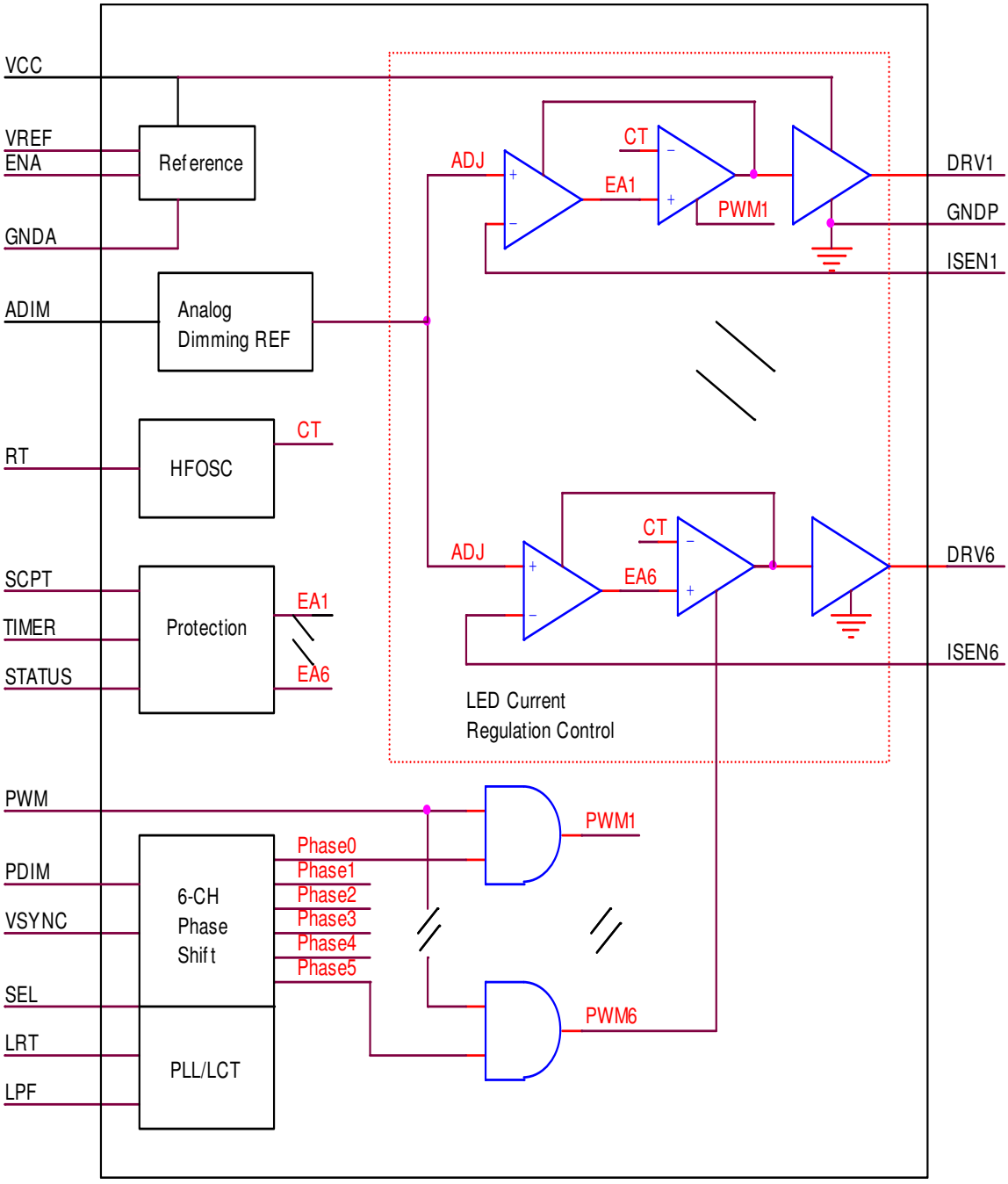


Figure 1

FUNCTIONAL DESCRIPTION

Refer to the Functional Block Diagram in Figure 1, Page 6.

The Reference block provides the bias current and low voltage supply for internal blocks.

The HFOSC (High-Frequency Oscillator) block generates a frequency for the switch mode balance control.

The LED Current Regulation Control block regulates the LED current for each string.

The PLL/LCT block provides the internal PWM dimming frequency and also supports the synchronization function. An external PWM signal can be applied to pin PWM to directly control the IC dimming function.

The 6–CH Phase Shift block provides an equal-phase-shift function among all activated strings during PWM dimming.

The Protection block provides the circuitry for LED short-circuit and MOSFET over-current protections and fault STATUS output.

Refer to the Typical Application Circuit in Figure 4, Page 10 for the operation of the DC/DC converter.

1.0. Enable

OZ9906 is enabled when the voltage at pin ENA is greater than approximately 2.0V. A voltage of less than approximately 1.0V disables the IC.

An under-voltage lockout protection feature is provided to both pin VCC and pin VREF and will disable the IC.

When voltage at pin VCC decreases below a threshold of approximately 6.5V, the IC drive outputs are disabled. The IC will resume operation once the voltage at pin VCC exceeds a threshold of approximately 6.8V.

When the voltage at pin VREF decreases below a threshold of approximately 3.5V, the IC drive outputs are disabled. The IC will resume normal operation once the voltage at pin VREF exceeds a threshold of approximately 3.8V.

Referring to Figure 2, the recommended turn-on sequence is VIN, VCC, VSYNC (if used), DIM (including PDIM, ADIM, PWM) followed by ENA. The recommended turn-off sequence is ENA followed by DIM signals, VSYNC (if used), VCC and VIN.

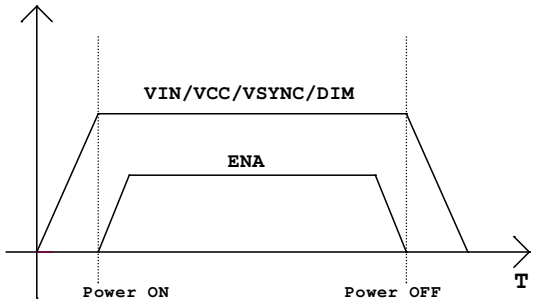


Figure 2

2.0. High Frequency Oscillator

The operation frequency of the switch mode balance control circuit is set by resistor R_{RT} connected between pins RT and GNDA. The typical operating frequency can be approximated by the following equation:

$$f_{OP}(kHz) = \frac{22{,}000}{R_{RT}(k\Omega)}$$

The frequency-spread range is approximately +/-3% of the typical operating frequency.

3.0. Current Regulation and Analog Dimming Control

Analog dimming is achieved by applying a voltage in the range of approximately 0.5V to 2.5V to pin ADIM. The corresponding LED current regulation level at pins ISEN1~ISEN6 is in the range of approximately 0.1V to 0.5V. The LED current can be approximated by the following equation

$$I_{LED}[mA] = \frac{V_{ADIM}[mV]}{5 \times R_{ISEN}[\Omega]}$$

$$(500mV \le V_{ADIM} \le 2500mV)$$

If the voltage applied to pin ADIM is greater than approximately 2.5V, the regulated reference

voltage (ADJ) at pins ISEN1~ISEN6 is fixed at approximately 0.5V. The LED current is approximated by the following equation:

$$I_{LED}[mA] = \frac{500}{R_{ISEN}[\Omega]}$$

If the voltage applied to pin ADIM is less than approximately 0.5V, the regulated reference voltage (ADJ) at pins ISEN1~ISEN6 is fixed at approximately 0.1V. The LED current is approximated by the following equation:

$$I_{LED}[mA] = \frac{100}{R_{ISEN}[\Omega]}$$

4.0. Dimming Control

OZ9906 supports both internal and external PWM dimming control.

4.1. Internal PWM Dimming Control

Internal PWM dimming control is achieved by applying DC voltage to pin PDIM.

Varying the DC voltage in a range of approximately 3.1V to 0.1V controls the panel brightness from 100% to 0% respectively.

The free-run PWM dimming frequency is set by resistor R_{LCT} connected between pins LRT and GNDA.

The typical free-run frequency can be approximated by the following equation:

$$f_{LFOSC}(kHz) = \frac{550}{R_{LRT}(k\Omega)}$$

4.1.1. Synchronized Internal Dimming Frequency

The internal PWM dimming frequency can be synchronized by applying an external signal to pin VSYNC. Components (R7, C9, C10) connected to pin LPF serves as the compensation function. To implement the internal dimming frequency synchronization function, the IC internal free-run PWM dimming frequency must be set lower than synchronization signal frequency.

The synchronized dimming frequency (F_{dim}) is set by the following equation:

$$F_{\text{dim}} = K \times F_{SYNC}$$

Where, F_{SYNC} is the synchronization signal frequency and K is determined by the setting of pin SEL.

K=1, if SEL=GNDA
K=32, if SEL= OPEN
K=128, if SEL=VREF

4.1.2. Phase-Shift Dimming Control

The IC provides a phase-shift function for PWM dimming operation. The number of phases is selectable from 2 to 6.

When all 6 LED strings are connected, each string is phase-shifted by 60 degrees.

Figure 3 illustrates the “on/off” PWM dimming waveforms for a 6-phase application.

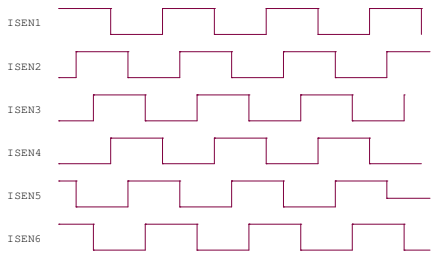


Figure 3

For 5-phase dimming control, ISEN6 is pulled to VREF and excluded from the control loop. The LED control loop consists of ISEN1~5 and DRV1~5.

For 4-phase dimming control, ISEN6 and ISEN5 are pulled to VREF and excluded from the control loop. The LED current control consists of ISEN1~4 and DRV1~4.

For 3-phase dimming control, ISEN2, ISEN4 and ISEN6 are pulled to VREF and excluded from the control loop. The LED control loop consists of ISEN1/3/5 and DRV1/3/5.

For 2-phase dimming control, ISEN1, ISEN3, ISEN5 and ISEN6 are pulled to VREF and excluded from the control loop. The LED control loop consists of ISEN2/4 and DRV2/4.

4.2. External PWM Dimming

An external PWM signal is applied to pin PWM to perform the dimming control function. Number of LED strings (≤6) is not limited.

Note that the phase-shift function is disabled when using external PWM dimming.

The logic high and logic low levels of the external PWM signal should be within a range of approximately 2.0V to 5.0V and 0.0V to 1.0V respectively.

5.0. Protection Features

5.1. Over-Current Protection (OCP)

OZ9906 provides OCP for the pins ISEN1~6 in the LED current balance circuit.

Refer to Figure 1 and Section 3.0 for the ADJ level. If the voltage at any ISEN pin (ISEN1~6) exceeds approximately 3 times the ADJ voltage, the corresponding DRV pin (DRV1~6) will be turned off. It will resume normal operation when next drive cycle begins. This feature protects the power MOSFET from being damaged by an excessive current.

5.2. LED Short-Circuit Protection (SCP)

OZ9906 provides a LED string short circuit protection feature. Pin SCPT can be set to limit the duty cycle of DRV. During normal operation, if the duty cycle of any DRV signal is less than the preset duty cycle threshold, the LED short circuit protection feature is activated and the delay timer is activated. Once the voltage at pin TIMER reaches a threshold of approximately 3.0V, the corresponding LED string(s) is considered “short-circuited”, and will be turned off and excluded from the control loop. The pin STATUS goes to logic LOW. If the short circuit condition disappears before the voltage at pin TIMER reaches the 3.0V threshold, TIMER will be discharged, and the SCP will be reset.

The time delay is determined by the following equation:

$$T_{TIMER}(S) = C_{TIMER}(uF)$$

The DRV duty cycle threshold is approximated by the following equation:

$$D(\%) = 78 \times V_{SCPT}(V)$$
$$(D \le 100)$$

To reset the IC, toggle pin ENA or pin VCC.

5.3. LED Open String

During normal operation, if the voltage at pins ISEN1~6 is less than 0.2*ADJ, pin TIMER is activated through charging the external capacitor C29. Once the voltage at pin TIMER reaches a threshold of approximately 3.0V, pin STATUS goes LOW to indicate a fault condition. The corresponding DRV is at logic High.

TYPICAL REFERENCE APPLICATION CIRCUIT

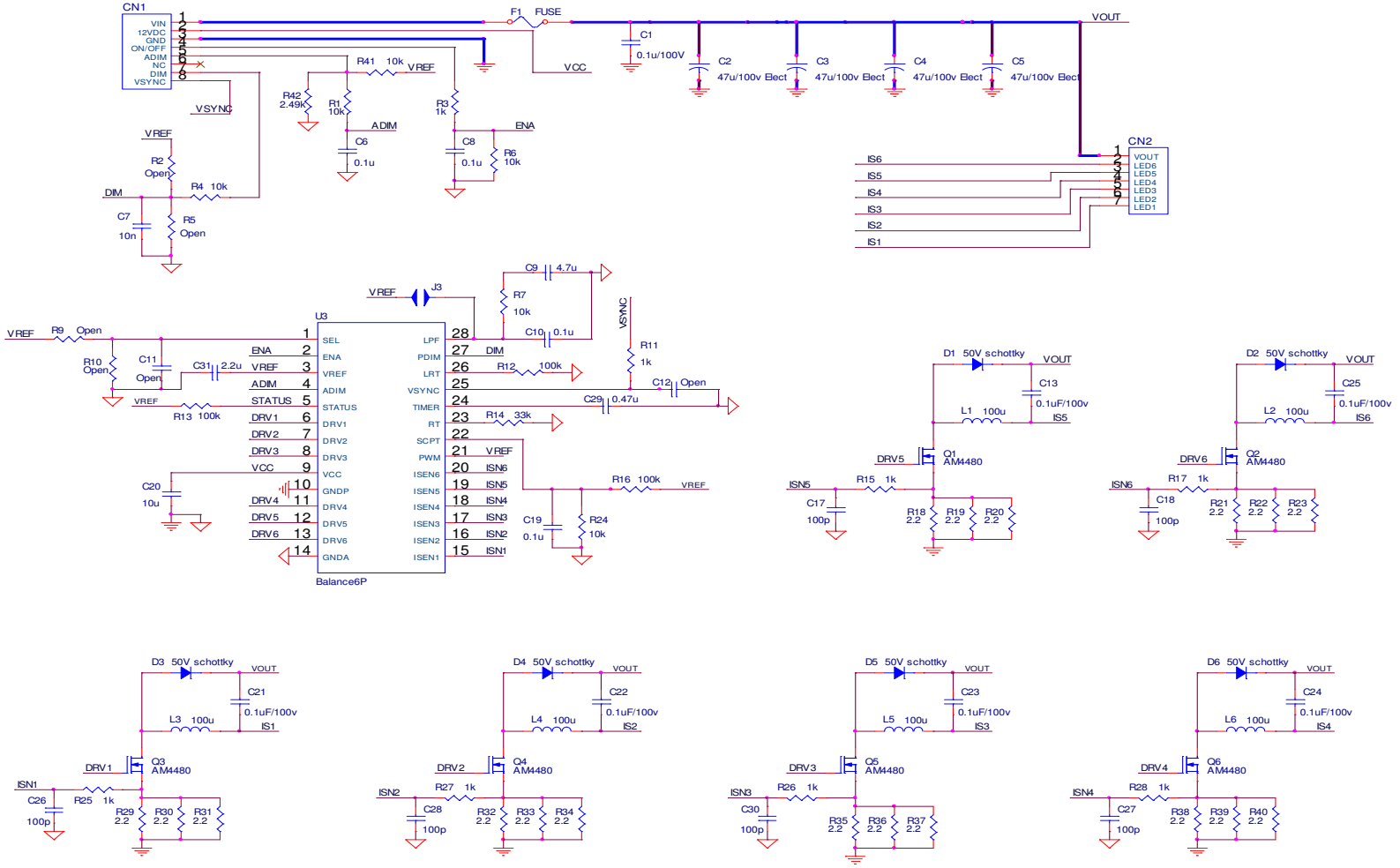


Figure 4

VLED: 30~40V (10LED/String)
ON/OFF: 2.0V - 5.0V, ON; 0V - 1.0V, OFF
DIM: Maximum brightness 3.1V
VSYNC: 50 or 60 Hz, Vp>2.5V
GNDP and GNDA should be connected together.

PCB Layout Guideline

OZ9906 is designed for high power LED applications. Therefore the PCB layout is important to ensure optimized system performance. Figures 4 and 5a/b, Pages 10 and 12 respectively, illustrate an example of a Typical Reference Application Circuit using a double layer PCB Layout for the 28-pin OZ9906. It is always recommended to separate the high frequency switching current from the low-level control signals. The high switching current may disturb other low-level signals in the protection circuitry. As a result, it may cause the IC functions abnormal. To avoid these issues, a few recommended guidelines for the PCB layout are listed below:

1. Use a separate plane for power GNDP and signal GNDA.
    - The ground for all power components must be connected together with the GNDP plane and then connected with the IC GNDP pin.
    - The ground for all signal components must be connected together with the GNDA plane near the IC and then connected to the GNDA pin of the IC.
    - Connect GNDP and GNDA planes together near the IC.
2. The first priority in the PCB layout is to select the ceramic capacitor (X5R, X7R) values (C20) for VCC decoupling greater than 2.2uF. The capacitors should be connected to VCC and GNDA pins using a wide/thick trace since it supports the internal IC drivers.
3. The second priority is to arrange the GNDP plane such that all the power components including the input capacitors and LED current sense resistors have a solid connection to the GNDP plane, especially on a single layer PCB.
4. The third priority is to keep all the drain areas of the balance MOSFET as far as possible from any small signal traces (ISEN, VSYNC) to avoid interference.
    - It is recommended to add a RC filter (1kΩ and 100pF) to each ISEN pin. The filter should be as close to its respective ISEN pin as possible.
    - If using the VSYNC function, it is also recommended to use a RC filter (10kΩ, 1nF for 60Hz) for the VSYNC signal. The filter should be as close as possible to the VSYNC pin.
5. The GNDA plane should be near the IC such that all small signal components have a short trace between the component and its respective IC pins.
    - Components connected to pins RT, DIM and other logic pins should be connected as close to their respective IC pins, while using pin GNDA for the ground connection.
6. Lastly, the DRV pins have a high switching frequency and drive the balance MOSFETs in a switching mode. The trace connection between the DRV pins and their corresponding balance MOSFET gate should be as short and wide as possible to reduce the wire resistance and inductance. If jumper wires are needed, it is recommended to use multiple jumper wires in parallel.

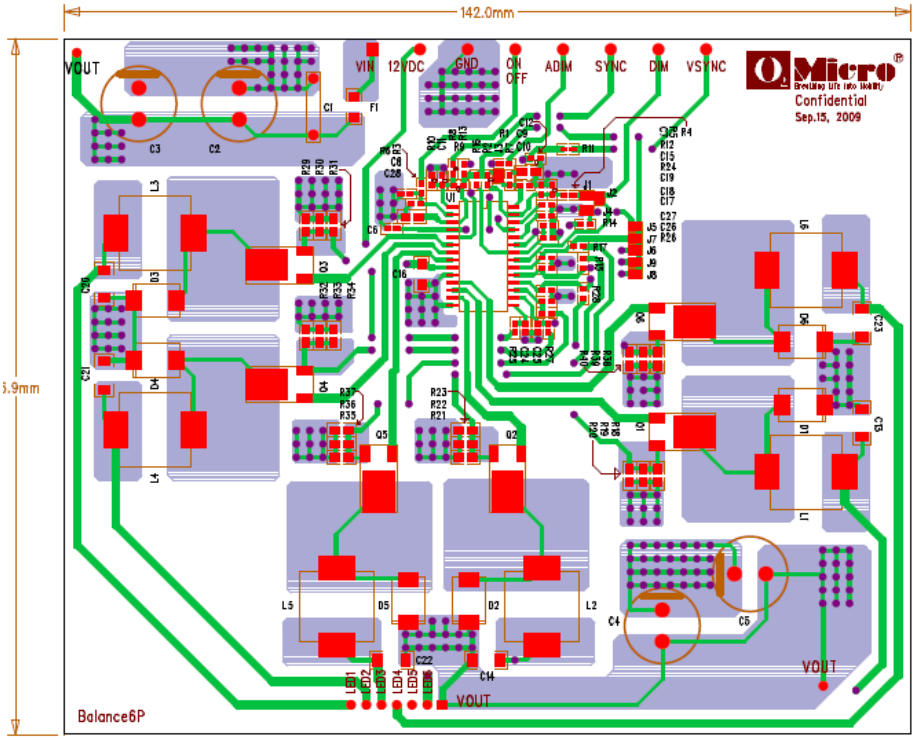


Figure 5a: PCB Top View

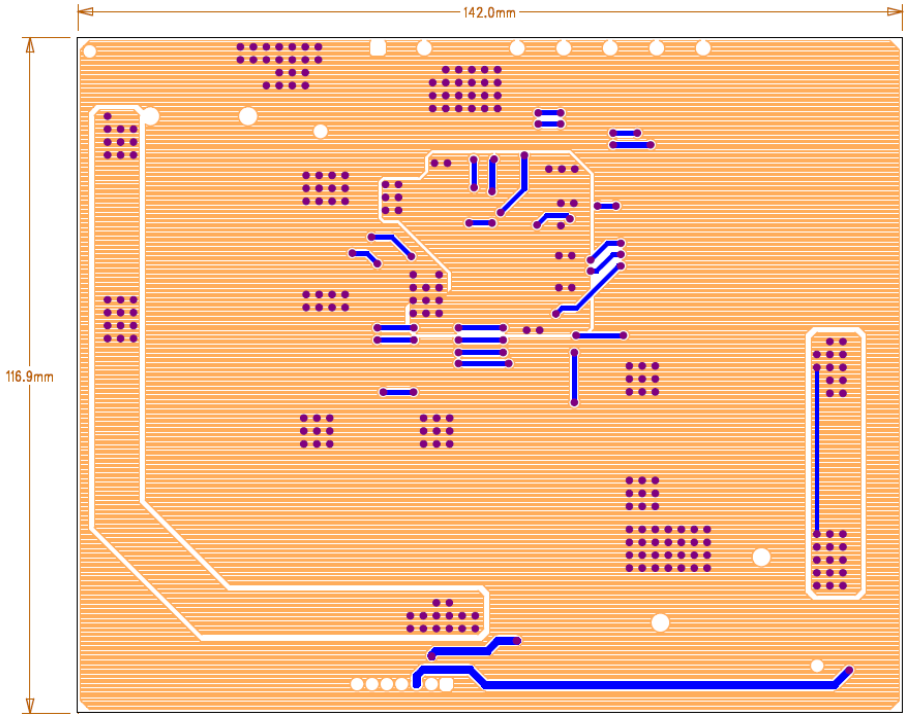
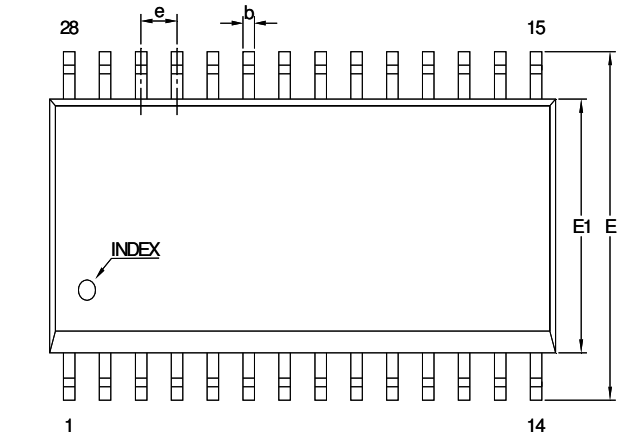
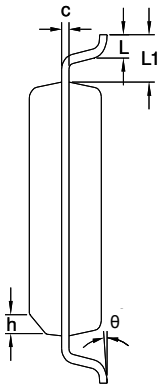
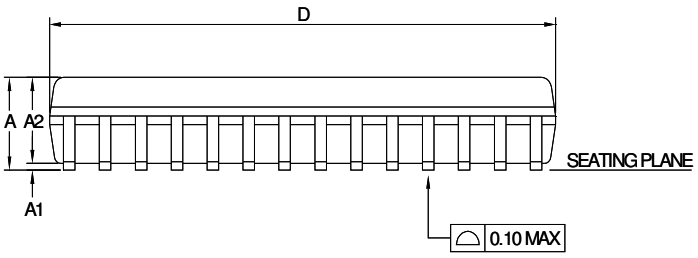


Figure 5b: PCB Bottom View

PACKAGE INFORMATION: 28-PIN SOP: OZ9906GN (300mil)







SYMBOL	DIMENSION (MM)		
	MIN	NOM	MAX
A	2.36	2.54	2.64
A1	0.10	0.20	0.30
A2	2.26	-	-
b	0.35	-	0.48
c	0.23	-	0.31
D	17.70	17.83	18.10
E	10.00	10.31	10.65
E1	7.40	7.50	7.60
e	1.27 BSC		
L	0.51	-	1.02
L1	1.40 REF		
h	0.25	-	0.75
θ	0°	-	8°

NOTE:
1. REFER TO JEDEC STD MS-013 AE
2. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER END. DIMENSION "E1" DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE

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