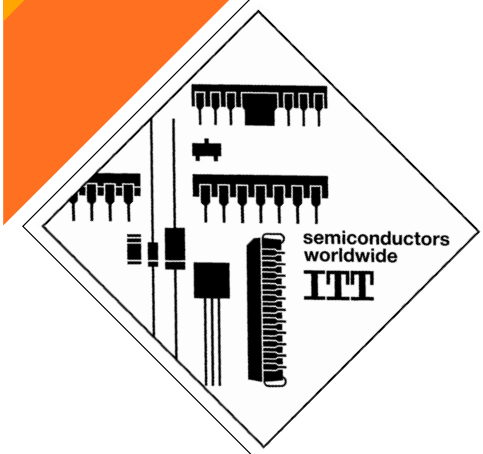

PRELIMINARY DATA SHEET

MSP 2410, MSP 2410 S
Multistandard
Sound Processors

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ITT Semiconductors

Contents

Multistandard Sound Processor

Note: This data sheet is valid for MSP 2410, Technical Code ≥ 09 and for TC 07. If not otherwise designated the pin numbers mentioned refer to the 44–pin PLCC package. For corresponding DIL package numbers please see pages 26 and 27.

1. Introduction

The MSP 2410 Multistandard Sound Processor is a CMOS circuit, housed in a 44–pin PLCC package. It is the successor of the MSP 2400. For differences between the MSP 2400 and the MSP 2410 please see Table 1–2. The MSP 2410 is designed to simultaneously perform digital demodulation and decoding of NICAM–coded TV stereo sound, as well as demodulation of FM–monoTV sound. Alternatively, two carrier FM systems according to the German terrestrial specs or the satellite specs can be processed with the MSP 2410. Since it is simple and economic to demodulate AM sound carriers with conventional sound–IF–mixing units, the AM demodulation feature of the MSP will seldom be used. However, for FM carrier detection in satellite operation the AM demodulation offers a powerful feature to calculate the carrier field strength, which can be used for automatic search algorithms. So the IC facilitates a first step towards multistandard capability with its very flexible application and may be used in TV–sets, satellite tuners and video recorders.

The MSP 2410 is available in 44–pin PLCC and in 40–pin DIL packages. There is also a 40–pin dual–in–line version, called MSP 2410 S, which is not provided for NICAM operations, but mainly for satellite applications. The IC's input signal consists of analog audio signals at intercarrier position and its output is up to three different audio baseband channels at the same time. Deemphasis filtering belongs to baseband processing and is therefore not performed in the MSP 2410. Some system parameters can be controlled by a microprocessor (CCU) via the IM–Bus, facilitating programmable quadrature mixers and filters. The MSP 2410 covers the sound processing of a wide range of TV–standards, of which some examples are listed in Table 1–1.

The MSP 2410 facilitates profitable multistandard capability, offering the following advantages:

– two selectable analog inputs (TV– and SAT–IF sources)

– Automatic Gain Control (AGC) for analog input: input range: 0.14 – 3 Vpp

– integrated 6 bit A/D converter

– all demodulation and filtering is performed on chip and is individually programmable

– simple realization of both digital NICAM standards (UK/Scandinavia) synchronization

– no external filter hardware is required

– only one crystal clock (18.432 MHz) is necessary

– Pay–TV for NICAM–mode

– FM carrier level calculation for automatic search algorithms and carrier mute function

– up to three different audio–channels available at the MSP's S–Bus output.

Table 1–1: European TV standards

TV–System	Position of Sound Carrier /MHz	Sound Modulation	Color System	Country
B/G	5.5/5.74	FM–Stereo	PAL	W. Germany
B/G	5.5/5.85	FM–Mono/NICAM	PAL	Scandinavia,Spain
I	6.0/6.552	FM–Mono/NICAM	PAL	UK
D,K	6.5	FM–Mono	SECAM	USSR
M	4.5	FM–Mono	NTSC	USA
Satellite Satellite	6.5 7.02/7.2	FM–Mono FM–Stereo	PAL PAL	Europe (ASTRA) Europe (ASTRA)

Table 1–2: Differences between MSP 2410 and MSP 2400

Feature	MSP 2400	MSP 2410
Pinning	see MSP 2400 data sheet, page 25 to 31	see MSP 2410 data sheet, page 25 to 36
IF–input Signal	AC: 0.6 to 2 V_{pp} DC: VREFTOP	AC: 0.14 to 3 Vpp DC: none
AGC Control	none; AD_CV = 0 Address of the AD_CV: HEXa = 0BF see MSP 2400 data sheet page 13, 14	by means of AD_CV Address of the AD_CV: HEXa = 0BB see MSP 2410 data sheet page 14, 15
IMREG1	12hex; MSP 2400 data sheet page 15	4hex; MSP 2410 data sheet page 17
IMREG2	0 ; MSP 2400 data sheet page 15	4hex; MSP 2410 data sheet page 17
FM–Sat–Coeff.	see MSP 2400 data sheet page 16	see MSP 2410 data sheet page 17, 18

2. Application of the MSP 2410

In the following a short overview about the two main TV sound standards, NICAM 728 and German FM–Stereo, demonstrates the complex requirements to a multistandard audio IC.

2.1. NICAM plus FM–Mono

According to the British, Scandinavian and Spanish TV–standards, in the near future high quality stereo sound will be transmitted digitally. The systems will allow two high quality digital sound channels to be added to the already existing FM channel. The sound coding follows the format of the so–called Near Instantaneous Companding System (NICAM 728). Transmission is performed using Differential Quadrature Phase Shift Keying (DQPSK). Table 2–1 gives some specifications of the sound coding (NICAM); Table 2–2 offers an overview of the modulation parameters.

In the case of NICAM/FM mode there are three different audio channels available at the chip's output (S–Bus, see section 3.2.1.): NICAM A,NICAM B and FM–mono. NICAM A and B may belong either to a stereo or to a dual language transmission. Information about operation mode and about the quality of the NICAM signal can be read by the CCU via the IM–Bus. In the case of low quality (high bit error rate) the CCU may decide to switch to the analog FM–mono sound.

Table 2–1: Summary of NICAM 728 sound coding characteristics

Characteristics	Values
Audio sampling frequency	32 kHz
Number of channels	2
Initial resolution	14 bit/sample
Companding characteristics	near instantaneous, with compression to 10 bits/sample in 32–samples (1 ms) blocks
Coding for compressed samples	2's complement
Preemphasis	CCITT Recommendation J.17 (6.5 dB attenuation at 800 Hz)
Audio overload level	+12 dBm0 measured at the unity gain frequency of the preemphasis network (2 kHz)

Table 2–2: Summary of NICAM 728 sound modulation parameters

Specification	**UK**	**Scandinavia/Spain**
Carrier frequency of digital sound	6.552 MHz	5.85 MHz
Transmission rate	728 kBit/s 1 part/million	
Type of modulation	Differentially encoded quadrature phase shift keying (DQPSK)	
Spectrum shaping	by means of Roll–off filters	
Roll–off factor	1.0	0.4
Carrier frequency of analog sound component (FM–mono)	6.0 MHz	5.5 MHz
Power ratio between vision carrier and analog sound carrier	10 dB	13 dB
Power ratio between analog and digital sound carrier	10 dB	7 dB

Table 2–3: Key parameters for German 2–carrier sound system

Sound Carriers	**Channel FM1**	**Channel FM2**
Intercarrier frequencies	5.5 MHz	5.7421875 MHz
Vision/sound power difference	13 dB	20 dB
Sound bandwidth	40 Hz to 15 kHz	
Pre–emphasis	50 µs	
Frequency deviation	±50 kHz	
Sound Signal Components		
Mono transmission	mono	mono
Stereo transmission	(L+R)/2	R
Dual sound transmission	language A	language B
Identification of Transmission Mode on Channel 2		
Pilot carrier frequency		54.6875 kHz
Type of modulation		AM
Modulation depth		50%
Modulation frequency		mono: unmodulated stereo: 117.5 Hz dual: 274.1 Hz

2.2. German 2–Carrier System (DUAL FM System)

Since September 1981, stereo and dual sound programs are being transmitted in Germany using the 2–carrier system. Sound transmission consists of the already existing first sound carrier and a second sound carrier additionally containing an identification signal. Some more details of this standard are given in Table 2–3. In the case of the FM–stereo mode at the MSP 2410 output (S–Bus, see section 3.2.1.) the demodulated channels FM1 and FM2 are available. On a separate output pin (PWM FM2) channel FM2, including identification signal, is available.

2.3. MSP 2410 in ITT's Digital Audio System

The MSP 2410 is designed to cooperate with ITT's Digital Audio System (Fig. 2–1). Its input is the analog sound IF signal coming from an analog quasi–parallel sound circuit. The output signal is conveyed digitally via S–Bus to the further components, which are as follows:

AMU 2481 VS

The Audio Mixer controls the desired sound sources, entering via the S–Bus (or PDM inputs) to MAIN and/or AUX channel. Since FM–channels, coming from the MSP 2410 have a sampling frequency of 64 kHz (→ one audio channel occupies two S–Bus channels), a sampling conversion to 32 kHz is performed in the AMU_VS. The AMU 2481 VS' main task is the selection of four S–Bus channels. This comprises the FM–sound dematrixing (if necessary) and the allocation of signals to the analog and digital output channels.

Further functions of the AMU 2481 VS are:

– all deemphasis types

– oversampled D/A–conversion for the SCART output.

ACP 2371

The hardware of this circuit largely corresponds to that of the AMU 2481 VS. However, the ACP 2371 is also equipped with integrated pulse–density–modulation converters.

The ACP 2371 contains the following signal inputs:

– 3 analog audio–baseband stereo pairs,

– one digital S–Bus input (4 channels)

and the following signal outputs:

– 2 controlled pairs for main speaker and head phone (MAIN/AUX) and

– one uncontrolled SCART output.

Via a further input (pilot) the ACP 2371 receives the identification signal of the second FM–carrier from the MSP 2410. This enables the ACP 2371 to determine certain identification values, which are used by the CCU to fix the actual operation mode.

The software functions of the ACP 2371 are:

– control of the tuning functions (volume, balance, treble and bass, stereo basewidth enlargement, pseudo–stereo, loudness)

– D/A–conversion with a signal–to–noise ratio of 85 dB at the output.

All components work with the 18.432 MHz clock, supplied by the MSP 2410. If the D2MAC chip DMA 2270 is also included in the system, it is possible to pass the DMA's system clock through the MSP 2410 to supply the whole audio system. All components are controlled by the central control unit (CCU 2070). Parameters, such as coefficients, increments etc., can be written to or read out of the corresponding ICs via the IM–Bus.The CCU decides about the operation mode (mono, stereo...) by periodically reading certain IM–Bus registers of the ACP (FM–stereo) or the MSP 2410 (NICAM) and evaluating them. For more information on communication between CCU and MSP 2410 see chapter 4. For more detailed information about ITT's audio systems see data sheet "TV Audio Systems".

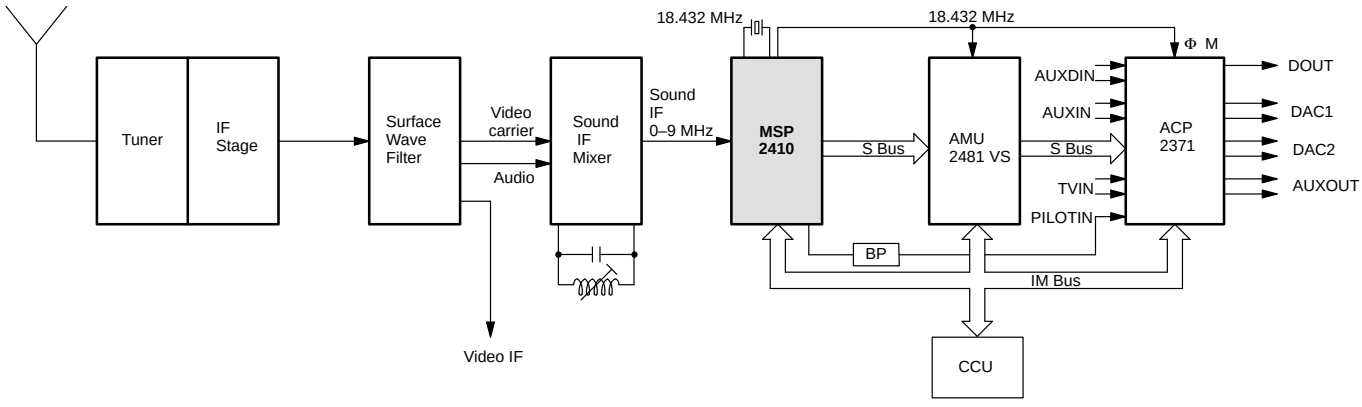


Fig. 2–1: MSP 2410 in the ITT digital audio system

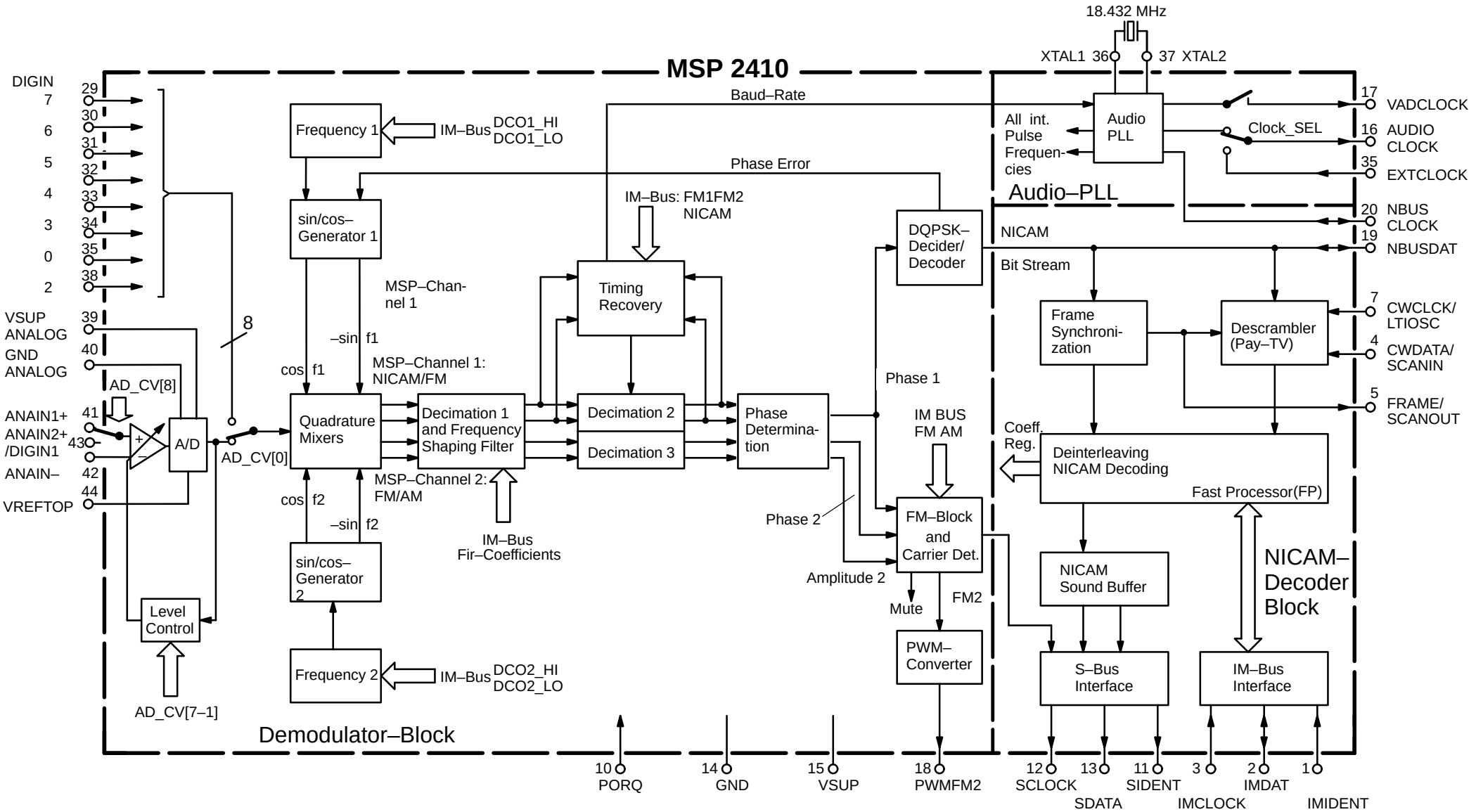


Fig. 3–1: Architecture of the MSP 2410 (pin numbers refer to PLCC version)

3. Architecture of the MSP 2410

Fig. 3–2 shows a simplified block diagram of the IC. Its architecture is split into three functional blocks:

1. Demodulator Part
2. NICAM Decoder Part
3. Audio PLL

3.1. Demodulator Block

Analog Sound IF – Input Section

The input pins 41, 42 and 43 offer the possibility to connect two different sound IF sources to the MSP 2410. By means of bit [8] of AD_CV (see Table 4–1) either terrestrial or satellite sound IF signals can be selected. The analog–to–digital conversion of the preselected sound IF signal is done by a 6–bit flash–converter, whose output can be used to control an analog automatic gain circuit (AGC), providing optimum level for a wide range of input levels.It is possible to switch between automatic gain control and a fixed (setable) input gain.

Quadrature Mixers

The digital input coming from the integrated A/D converter or alternatively from an external AD–CV may contain audio information at a frequency range of theoretically 0 to 9 MHz corresponding to the selected standards. By means of two programmable quadrature mixers two different audio sources, for example NICAM and FM–mono, may be shifted into baseband position. The 4 output channels of the mixers are to be interpreted as two main channels, each carrying a complex signal pair. In the following the two main channels are provided to process either:

– NICAM (channel 1) and FM mono (channel 2) simultaneously or alternatively

– FM2 (channel 1) and FM1 (channel 2).

Two independent digital oscillators are provided to generate two pairs of sin/cos–functions. Two programmable increments, to be divided up into Low– and High Part, determine the oscillators' frequency, which corresponds to the frequency of the desired audio carrier. The upper oscillator can be controlled by a correction increment and can manage synchronous demodulation in the case of NICAM operation mode. In section 4., format and values of the increments are listed.

Filtering

By means of decimation filters the sampling rate is reduced from 18.432 to 4.608 MHz. Then data shaping and/or FM bandwidth limitation is performed by a linear phase FIR–filter, which is multiplexed to process four channels. Just like the oscillators' increments the filter coefficients are programmable and are written into the IC by the CCU via the IM–Bus. Thus, for example, different NICAM versions can easily be implemented. Two not necessarily different sets of coefficients are required, one for channel 1 (NICAM or FM2) and one for channel 2 (FM1=FM–mono). In section 4.2.3. several coefficient sets are proposed.

Since both MSP channels are designed to process the German FM Stereo System with the same FIR coefficient set (despite 6 dB power level difference of the two sound carriers), the MSP channel 2 has an internal overall gain of 6 dB. To process two cariers of identical power level these 6 dBs have to be taken into account by decreasing the values of the channel 2 coefficient set, which has already been done in table 4–7.

Timing Recovery (not for S–Version)

To detect the original NICAM data stream another decimation to the symbol rate which is 364 kbaud/s has to be performed. This process is accomplished by a block called 'Timing Recovery', which locks the decimation frequency to the transmitted symbol–rate.

For analog sound signals an integer decimation to 384 kHz is provided.

Phase Determination

For the reconstruction of the NICAM phase shifts as well as for the FM demodulation it is advantageous to convert the two complex signal pairs from carthesic into polar coordinates,which is done by a multiplexed cordic circuit.

DQPSK Decider/Decoder (not for S–Version)

The next step to reconstruct the serial NICAM data stream is to evaluate the phase shifts, which can be transformed directly into a dibit according to a table defined by the NICAM system.

FM Block

After obtaining the phase in the phase determination block FM demodulation is completed by differentiation of the FM sound samples in the FM part. Further filtering and decimation to 64 kHz, which is required to convey FM sound via the S–Bus to the AMU, is processed in this block, too. As a consequence of the 64 kHz sampling frequency, two S–Bus channels are required for each FM sound channel instead of the default frequency of 32 kHz. Conversion to 32 kHz is performed in the AMU (see data sheet AMU 2481 VS) or alternatively in the ACP.

To facilitate the check for FM–stereo identification signal, the complete FM2 channel is converted into a pulse wide modulated stream and led to the output pin PWM FM2.

MSP–Mute Function in the Dual Carrier FM Mode

To prevent noise effects or FM identification problems in the absence of one or both FM carriers the MSP2410 offers a carrier detection feature, which must be activated

by means of AD_CV[9], see section 4.2.2. If no FM carrier is available at the MSP channel 1 (= FM2), the corresponding S–Bus samples (3 and 4) and the PWMFM2 output are muted. If no FM carrier is available at the MSP channel 2 (= FM1/mono), the corresponding S–Bus samples (1 and 2) are muted.
The Mute Function is not recommended for the Satellite-mode.

3.2. NICAM Decoder Part (not for S–Version)

Frame Synchronization

Since the serial NICAM bit stream is partitioned into frames of 728 bit, the receiver has to synchronize to this frame structure. Each frame begins with the 8 bit Frame Alignment Word (FAW). By means of a FAW–correlator and a so–called Frame Fly–Wheel the system locks to the frame sequence. At the output pin FRAME there is a 1 kHz signal, which is low for a sequence of 8 bit and high for 720 bit.

Descrambler

In the NICAM transmitter the serial data stream is scrambled for energy dispersal purposes. The scrambling is done synchronously with the frame multiplex. The frame alignment word is not scrambled, because it is used, as already mentioned, to synchronize the pseudo–random sequence generator used for descrambling in the receiver.

For default NICAM transmission the pseudo–random sequence generator in the descrambler has to be initialized after each FAW with the same starting value, which is done automatically in the MSP 2410.

Fast Processor: Deinterleaving and NICAM Decoding

The NICAM decoding, i.e recovering of the scaling factors, expanding the audio samples from 10 back to 14 bit and error correction, is now done in a RISC processor, which is implemented on chip. The so-called FP (Fast Processor) also performs the deinterleaving function in order to put the data bits into the original sequence again.

Another important task of the FP is to link all chip–internal registers to the IM–Bus registers of the MSP 2410 (more about this in the following sections).

To facilitate the Central Control Unit CCU to switch the TV set to the transmission operation mode, control information on NICAM operation mode and bit error rate is supplied by the FP via the IM–Bus.

After decoding, resulting in two sound channels carrying either stereo or bilingual sound, the audio samples have to be buffered in the so–called sound buffer block. Here they are written to the S–Bus to be conveyed to the AMU in a 32 kHz rate.

3.2.1. S–Bus Interface

Digital audio information provided by the MSP 2410 is serially transmitted to the AMU via the S–Bus.
The MSP 2410 has the master function.

The S–Bus interface consists of three pins:

1. S–DATA:
Four channels (4*16 bits) per sampling cycle (32 kHz) are transmitted. The two possible NICAM channels each require one S–Bus channel, whereas each FM channel requires two S–Bus channels.

2. S–CLOCK:
Gives the timing for the transmission of S–DATA (4.608 MHz).

3. S–IDENT:
After 64 S–CLOCK cycles the S–IDENT determines the end of one sampling period.

According to the two possible operation modes there are two ways to switch the output channels to the S–Bus, which is done by the S–Bus setting bit [10] of the control word MODE_REG (see 4.2.2.; Table 3–1). A precise timing diagram of the S–Bus is shown in Fig. 3–3.

In the case of D2MAC operation mode of the TV set the MSP 2410 S–Bus pins have to be switched to the tristate position by means of MODE_REG[11] (see 4.2.2.).

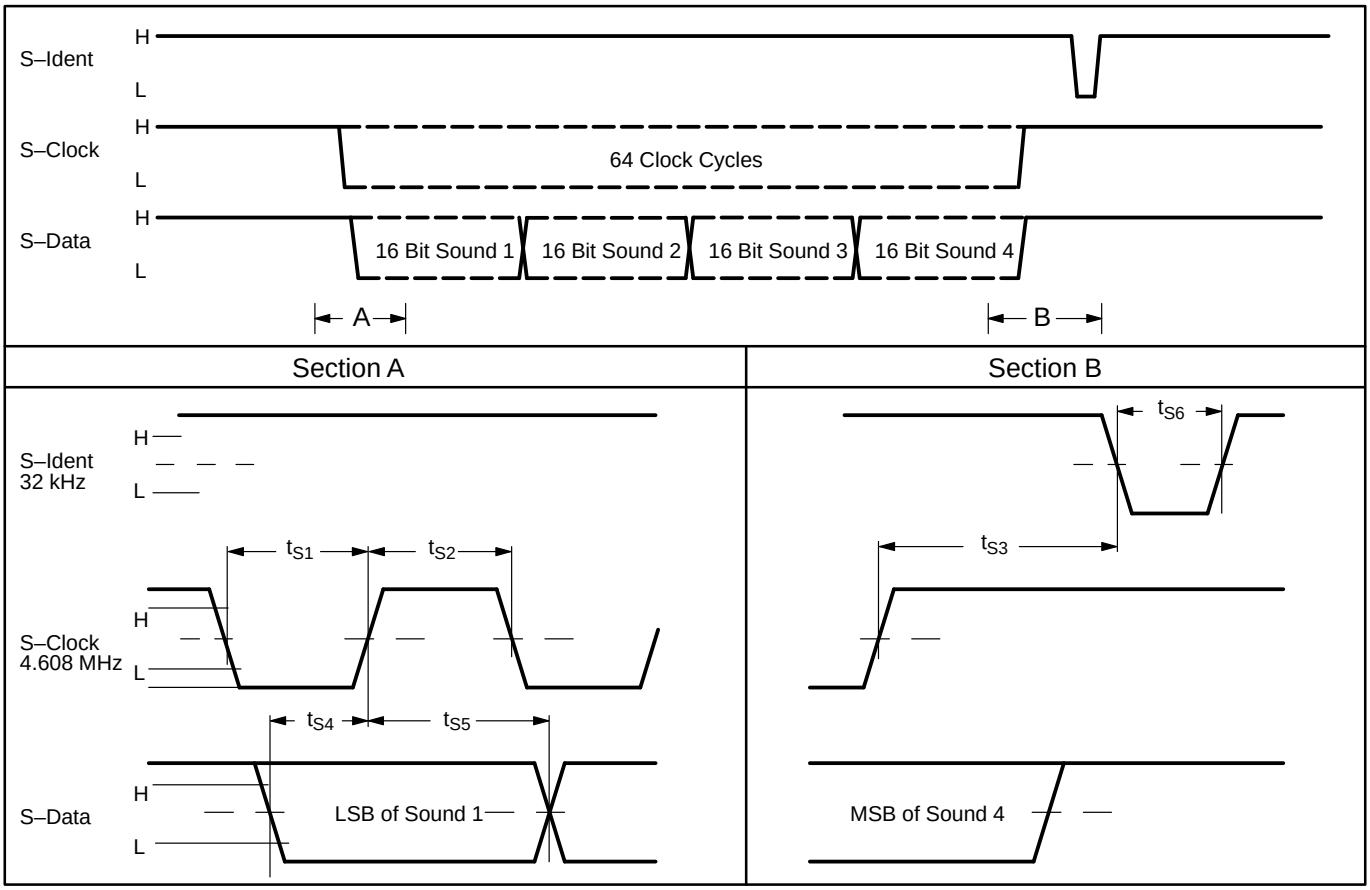


Fig. 3–3: S–BUS waveforms

Table 3–1: S–bus channel selection

S–Bus Setting in Mode_reg	Mode	Sample 1 MSP–CH2	Sample 2 MSP–CH2	Sample 3 MSP–CH1	Sample 4 MSP–CH1
0	NICAM and Analog Mono	FM mono	FM mono	NICAM L/A	NICAM R/B
1	Dual Carrier FM: – German terres–trial system – SAT	 FM1 FM–L/A	 FM1 FM–L/A	 FM2 FM–R/B	 FM2 FM–R/B
FM–signals in AMU and ACP available at		PDM1		PDM2	

3.2.2. IM–Bus Interface

The IM–Bus was designed by INTERMETALL to control the DIGIT 2000 chip set with a central control unit (CCU). Via the IM–Bus the CCU can write data to the ICs or read data from them by addressing special register locations inside each chip with a unique 8–bit address. This means that the CCU acts as a master whereas all controlled ICs are slaves. The average bit rate of the IM–Bus is about 100 kbit/s. The IM–Bus consists of three lines for the signals Ident (ID),Clock (CL) and Data (D). Ident and Clock are unidirectional from the CCU to the slave ICs, Data is bidirectional.

The IM–Bus interface of the MSP 2410 consists of 6 IM–Bus registers, each with its own 8–bit device address (Table 3–2).The user has to distinguish between the 6 IM–Bus registers and several MSP 2410 internal registers, which are provided for system parameters.

Values for these internal registers are transferred into the FP–processor via IM–Bus and IM–Bus registers, to be temporarily stored in its RAM, while the RAM ad-

dresses also have to be transmitted. From these RAM locations they are automatically conveyed by the FP to the corresponding internal registers triggered by a load command coming from the CCU (see section 4.4.4.).

Addressing the READ_ADR and DATA triggers the FP–IM–Bus routine to read in and to decode address or data by means of a so–called scheduler.

A first functional overview of the above registers is given in the following explanations; precise syntax protocols are listed in section 4.4.

– WRITE_ADR:
  This IM–Bus register is used to temporarily store a 12–bit address to define a RAM location inside the FP; besides this the 12 bits also carry an information for the FP, whether data to be written into the chip are 8– or 12–bit data.

– READ_ADR:
  This IM–Bus register is used to temporarily store a 12–bit address to define a RAM location inside the FP. While the FP reads the address and transfers the desired value to the DATA register, the Busy Bit of STATUS is set to high level.

– DATA:
  After transmitting the address A2, the next 8 bits are either loaded (in the case of WRITE_ADR) into DATA or read out of DATA (in the case of READ_ADR).

– STATUS:
  Before starting any IM–Bus activity the CCU has to check Bit[2] of the STATUS_Word, which must be interpreted as a Busy–Flag. IM–Bus activities are only accepted by the MSP 2410 if this bit is reset. Apart from this, a 12–bit word can be read out of the MSP 2410 by means of STATUS:

  8 bit [0 = LSB] – [7] via DATA (see 4.4.3)
  4 bit [8] – [11 = MSB] via STATUS:
  [3] of status = [11] of 12 bit word
  [4] of status = [10] of 12 bit word
  [5] of status = [9] of 12 bit word
  [6] of status = [8] of 12 bit word

  This additional feature is only necessary for checks of the FP hardware of the MSP.

– CONTROL:
  This address is not relevant for the user.

– EXT_ADR:
  Into this register a 12–bit data word can be written by the CCU without triggering the FP–IM–Bus routine. To activate the FP to write the value into the RAM location addressed by WRITE_ADR, a dummy 8–bit data word has to be sent to DATA.

A precise timing diagram of the IM–Bus is given in Fig. 3–4.

Table 3–2: IM–Bus register and its addresses

IM–Bus Register	Address	Direction	Word length	Scheduler
WRITE_ADR	A0	CCU → MSP	16*	no
READ_ADR	A1	CCU → MSP	16*	yes
DATA	A2	CCU ↔ MSP	8	yes
STATUS	A3	MSP → CCU	8	no
CONTROL	A4	CCU → MSP	16*	no
EXT_ADR	9F	CCU → MSP	16*	no
*= The 4 MSBs must always be set to 0.				

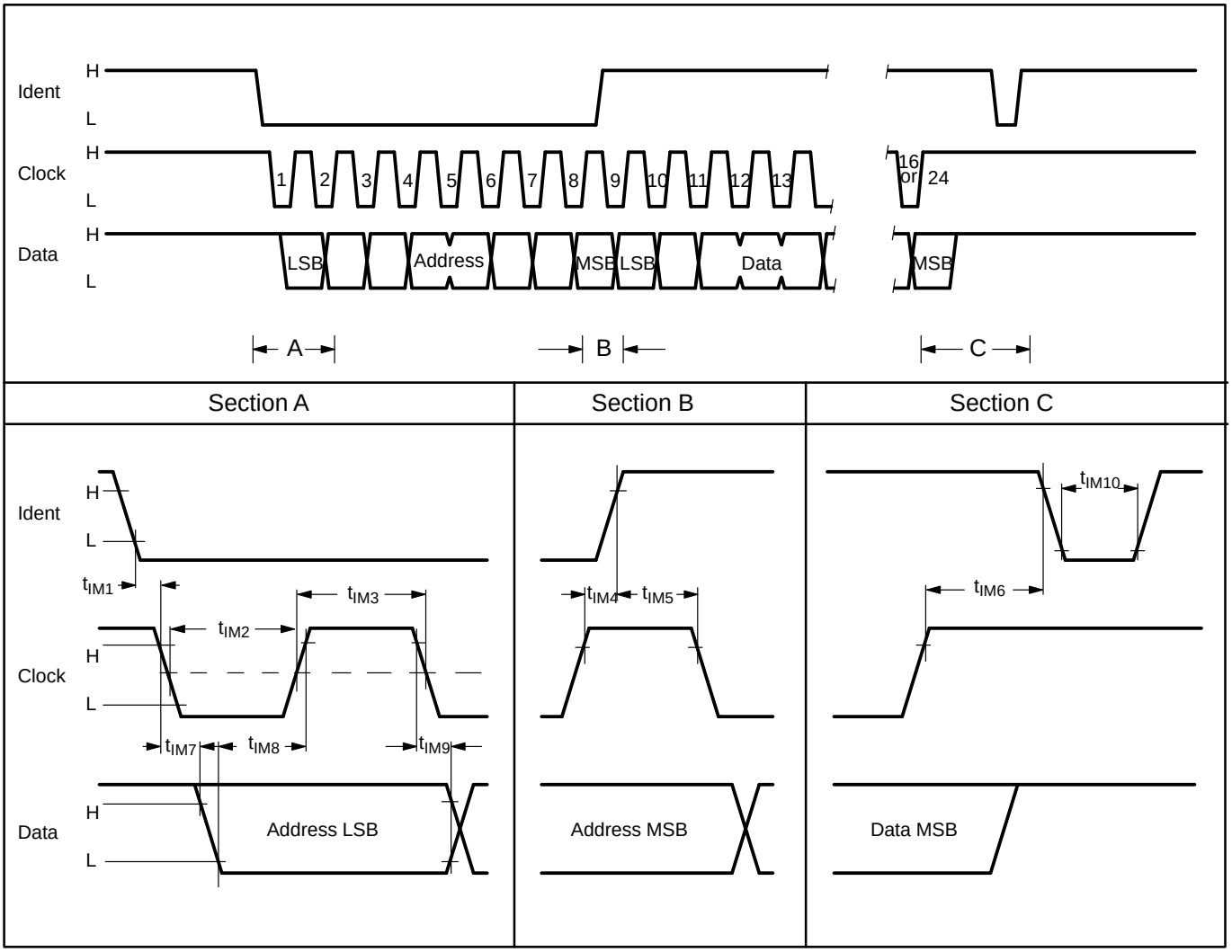


Fig. 3–4: IM–Bus waveforms

3.2.3. N–Bus Interface (not for S–Version)

The N–Bus interface can be used as an input or an output, to be switched by bit[5] of 'MODE_REG' (see section 4.2.2.). It consists of two lines, N–data and N–clock.

1. Output:
The pure NICAM_728 data stream is available together with a 728 kHz clock signal for the purpose of data transmission.

2. Input:
An external NICAM_728 bit stream, accompanied by an external clock signal can be processed instead of the internal generated stream.

N–Bus signals are based on TTL–levels. Data are latched with the falling clock edge.

3.2.4. Pay–TV Interface (not for S–Version)

The MSP 2410 facilitates the reception of encrypted NICAM sound, which is provided by Pay–TV systems. By means of bit 1 of the control word 'MODE_REG' the operation mode 'PAY–TV' can be activated. The MSP 2410 inherent descrambler generally uses a 9–bit start sequence, which initializes a pseudo random sequence generator each ms. In normal operation mode the 9–bit sequence exists of 9 bits having each high level, which are loaded automatically into the descrambler's shift register. In the Pay–TV mode these bits have to be loaded via the two pins 4 (CW–DATA) and 7 (CW–CLOCK) into the mentioned shift register. The time window to load one complete 9–bit sequence is given by the high time of the frame signal which is available on pin 5. It is not necessary to load a new sequence at each ms, because if no new sequence has been transmitted, the old one is saved. If less than 9 new bits at each ms are loaded, one has to consider that any new incoming bit shifts the old ones by one position inside the shift register. A complete timing diagram is illustrated in Fig. 3–5.

3.3. Audio PLL and Crystal Specifications

The MSP 2410 requires a 18.432 MHz (10 pF, parallel) crystal. The clock supply of the whole system depends on the MSP 2410 operation mode:

1. NICAM and FM_mono:
An integrated clock PLL uses the 364 kHz baud–rate, accomplished in the timing recovery block, to lock the system clock to the bit rate respective 32 kHz sampling rate of the NICAM transmitter. As a result, the whole audio system is supplied with a controlled 18.432 MHz clock. In this case the clock output VADCLOCK, which is provided for any external A/D converter, and the AUDIOCLOCK, which is provided for the remaining components, are identical.

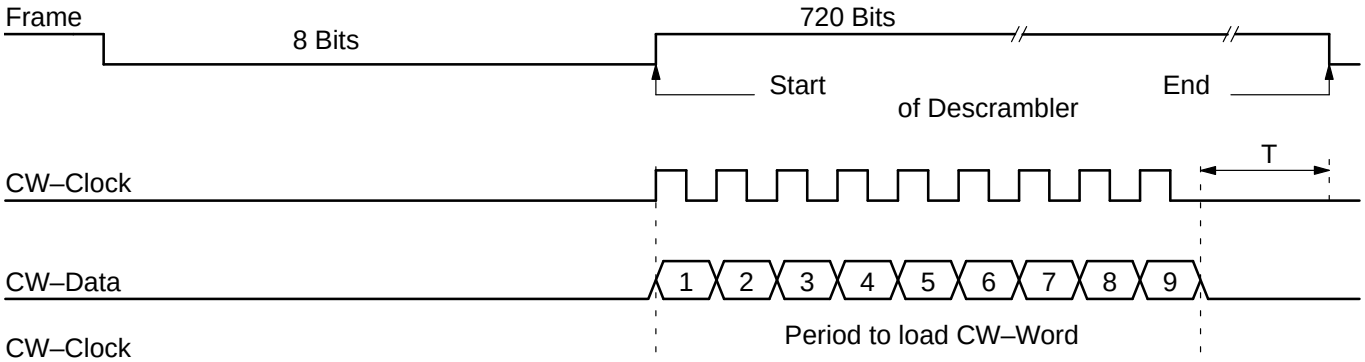
2. FM–Stereo:
Now the system clock runs free on the crystal's 18.432 MHz. VADCLOCK and AUDIOCLOCK are identical, too.

3. D2–MAC operation:
In this case the system clock is supplied by the D2–MAC chip. This means that the DMA's clock is passed through the MSP 2410 (see section 3.2.1). All audio components except the MSP and an external A/D–CV receive the DMA system clock via AUDIOCLOCK.

Remark on using the crystal:
External capacities of 1.5 to 10 pF at each crystal pin to ground are required. They are necessary to tune the open–loop frequency of the internal PLL and to stabilize the frequency in closed–loop operation. The higher the capacitors, the lower the clock frequency results. Please strive for the centre of the tolerance range between 18.433 and 18.431 MHz.

3.4. Operation with External System Clock

For pure FM–satellite operation in combination with an ITT DMA–processor the MSP2410(S) might be used without its own crystal. In this case the DMA's 18.432 MHz clock is fed capacitively into pin 36 (XTAL1) of the MSP, whereby the serial capacitor must be 1 nF. Please note that NICAM is not possible in this operation mode.



CW–Clock
Min: 10 kHz
Max: 4 MHz T ≥ 7E–6 s

Fig. 3–5: Timing for Pay–TV signals

4. Initializing and Programming the MSP 2410

The IC MSP 2410 consists of two main parts. These are the DQPSK–Demodulator (‘internal’) and the FAST PROCESSOR (FP) performing the NICAM decoding. Both require some parameters that are transferred from the CCU into the Fast Processor RAM via the IM–Bus, in the course of which the RAM addresses listed below have to be used.

Parameters provided in the demodulator part are temporarily stored in a certain area of the FP RAM and then transferred blockwise (except for FIR–parameters) to the internal write registers by transmitting a kind of start instruction to the FP (see section 4.4.4).

Values of internal read registers are written periodically into corresponding FP RAM positions. If required, access to these data is possible via the IM–Bus.

4.1. Write Registers: Table and Addresses

In Table 4–1 all Write Registers are listed. In the following, the register and its contents are named identically.

All data, except for FIR_REG_1/2 data, which are transferred to MSP 2410 are stored at well defined RAM positions inside the FP. To place them correctly each data word must be preceded by an address word (HEXa; Table 4–2).

Table 4–1: MSP 2410 write registers

Register	Function	Required Bits
FAWCT_SOLL FAW_ER_TOL	see 4.2. see 4.2.	8 bit 8 bit
AD_CV	input selection, configuration of AGC and Mute Function and selection of A/D–converter: see section 4.2.1.	10 LSBs of 12 bits
AUDIO_PLL	audio PLL in case of NICAM operation mode: 0 always open; 1 to be closed = default	LSB of 8 bits All other bits = 0
FIR_REG_1 FIR_REG_2	serial shift register for 6 · 8 bit, filter coefficient channel 1 (48 bit) serial shift register for 6 · 8 bit, + 2 · 12 bit off set (total 72 bit) see section 4.2.3.	6 · 8 bit 9 · 8 bit
MODE_REG DCO1_LO DCO1_HI DCO2_LO DCO2_HI	mode register (see section 4.2.1.) increment channel 1 Low Part (see section 4.2.3.) increment channel 1 High Part increment channel 2 Low Part increment channel 2 High Part	12 bit 12 bit 12 bit 12 bit 12 bit

Table 4–2: Addresses for write registers; bits [15] to [12] are always “0”; HEXi only for test purposes

Register	MSB Bit LSB												HEXi	HEXa
	11	10	9	8	7	6	5	4	3	2	1	0		
FAWCT_SOLL	0	0	0	1	0	0	0	0	0	1	1	1	20	107
FAW_ER_TOL	0	0	0	1	0	0	0	0	1	1	1	1	21	10F
AD_CV	0	0	0	0	1	0	1	1	1	0	1	1	17	0BB
AUDIO_PLL	0	0	1	0	1	1	0	1	0	1	1	1	5A	2D7
FIR_REG_1	0	0	0	0	0	0	0	0	0	0	0	1	00	001
FIR_REG_2	0	0	0	0	0	0	0	0	0	1	0	1	00	005
MODE_REG	0	0	0	0	1	0	0	0	0	0	1	1	10	083
DCO1_LO	0	0	0	0	1	0	0	1	0	0	1	1	12	093
DCO1_HI	0	0	0	0	1	0	0	1	1	0	1	1	13	09B
DCO2_LO	0	0	0	0	1	0	1	0	0	0	1	1	14	0A3
DCO2_HI	0	0	0	0	1	0	1	0	1	0	1	1	15	0AB

4.2. Write Registers: Functions and Values

In the following, the functions of some registers are explained and their (default) values are defined:

– FAWCT_SOLL, FAW_ER_TOL: (not for S–Version)
To synchronize to the frame structure of the NICAM bit stream, the FP checks the data for FAWs. After having captured the first one, the FP continues to check for n frame periods. On having found at least n–m FAWs after this period, the frame synchronism is achieved and the FP switches to active NICAM–decoding. The value for n has to be loaded into FAWCT_SOLL; the one for m into FAW_ER_TOL.
Proposal : n=12; m=2

4.2.1. Setting of Parameter AD_CV [11:0]:

AD_CV [0]: Selection of A/D converter
0 internal
1 external (test)

AD_CV [6:1]: Reference level in case of Automatic Gain Control = on, see Table 4–3. Constant gain factor when Automatic Gain Control = off, see Table 4–4.

AD_CV [7]: Determination of Automatic Gain or Constant Gain. Please consider for both cases:
Minimum gain: 3 dB
Maximum gain: 20 dB
0 = constant gain
1 = automatic gain

AD_CV [8]: Selection of analog input
0 = ANALOG IN1
1 = ANALOG IN2

AD_CV [9]: MSP–Mute Function
0 = off: no mute in any case
1 = on: mute as described in section 3.1.

AD_CV[10]: FIFO–Watchdog (not of interest for the customer)
0 = on: default
1 = off (for testing)

AD_CV[11]: Must be 0

Table 4–3: Reference values for active AGC (AD_CV[7]=1)

Application	Input Signal Contains	AD_CV [6:1] Ref. Value	AD_CV [6:1] in integer	Range of Input Signal at pin 41 or 43
Terrestrial TV	2 FM Carriers or 1 FM and 1 NICAM Carrier	101000	40	0.14 – 3 V_{pp} *)
SAT	1 or more FM Carriers	100011	35	0.14 – 3 V_{pp} *)
NICAM only	1 NICAM Carrier only	010100	20	0.07 – 1.0 V_{pp}

*) : For signals above 1.4 Vpp the minimum gain of 3 dB is switched. Internal overflow protected structures work properly up to more than 3 Vpp, however.

Table 4–4: AD_CV parameters for constant input gain (AD_CV[7]=0)

Step	AD_CV [6:1] Constant Gain	Gain	Input Level at pin 41 or 43
0	000000	3.00 dB	max. 3 Vpp
1	000001	3.85 dB	
2	000010	4.70 dB	
3	000011	5.55 dB	
4	000100	6.40 dB	
5	000101	7.25 dB	
6	000110	8.10 dB	
7	000111	8.95 dB	
8	001000	9.80 dB	
9	001001	10.65 dB	
10	001010	11.50 dB	
11	001011	12.35 dB	
12	001100	13.20 dB	
13	001101	14.05 dB	
14	001110	14.90 dB	
15	001111	15.75 dB	
16	010000	16.60 dB	
17	010001	17.45 dB	
18	010010	18.30 dB	
19	010011	19.15 dB	
20	010100	20.00 dB	min. 0.14 Vpp

4.2.2. Control Register 'MODE_REG'

The register 'MODE_REG' contains the control bits determining the operation mode of the MSP 2410; Table 4–5 explains all bit positions.

Comment on S–Bus setting: According to this control bit the 4 samples of the S–Bus are provided for the signals, as shown in Table 3–1.

Table 4–5: Control word 'MODE_REG': all bits are "0" after power–on–reset

Bit	Function	Comment	Definition	Recommendation
[0]	Testbus	Not of interest for customers	1 = MSBs / 0 = LSBs	1
[1]	PAYTV_EN	PAY–TV	on = 1 / off = 0	0
[2]	DESCR_DIS	Descrambler	on = 0 / off = 1	0
[3]	CLOCK_SEL	Audio system clock	0: MSP Clock 1: Ext. clock (D2MAC)	0
[4]	VAD_CLOCK	Clock, to drive ext. AD–CV	0: on 1: off	1
[5]	N_BUS	Selection of N–Bus mode	0: output 1: input (Test)	0
[6]	NICAM	MSP channel 1:	1: NICAM 0: FM (always for S–version)	X
[7]	FM1 FM2	MSP channel 1:	1: FM 0: NICAM	X

Bit	Function	Comment	Definition	Recom-mendation
[8]	FM AM	MSP–channel 2:	0: FM 1: AM	0
[9]	Test FIR	Test switch ROFITST	0/Test=1	0
[10]	S–Bus Setting		0: NICAM/Analog Mono 1: Two Carrier FM	X
[11]	S–Bus Mode		0: Tristate 1: Active	1
X: Depending on mode				

4.2.3. FIR–Parameter

Every time an 8–bit FIR_REG_1/2 value is written into the MSP 2410, the FP software transfers it bit–serially into one of the two FIR–Registers.

The following data values (see Table 4–7) are to be transferred **8 bits at a time:**

Note: These sequences must be obeyed (Table 4–6).

Table 4–6: Loading sequence for FIR–coefficients

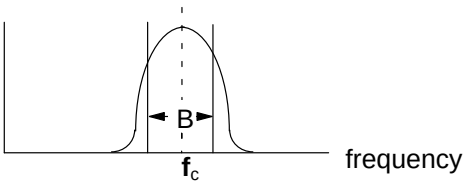
WRITE_ADR = FIR_REG_1(Channel 1: NICAM/FM2)			
No.	**Symbol Name**	**Bits**	**Value**
1	NICAM/FM2_Coeff. (5)	8	see Table 4–7.
2	NICAM/FM2_Coeff. (4)	8	
3	NICAM/FM2_Coeff. (3)	8	
4	NICAM/FM2_Coeff. (2)	8	
5	NICAM/FM2_Coeff. (1)	8	
6	NICAM/FM2_Coeff. (0)	8	

WRITE_ADR=FIR_REG_2 (Channel 2: FM1/FM mono)			
No.	**Symbol Name**	**Bits**	**Value**
1	* IMREG1 (8 LSBS)	8	4 HEX
2	* IMREG1/2 (4 MSBs / 4 LSBs)	8	40 HEX
3	* IMREG2 (8 MSBs)	8	0 HEX
4	FM_Coef (5)	8	see Table 4–7.
5	FM_Coef (4)	8	
6	FM_Coef (3)	8	
7	FM_Coef (2)	8	
8	FM_Coef (1)	8	
9	FM_Coef (0)	8	
* IMREG_1/2: Two 12–bit off–set constants			

IMREG1 and –2 are used to compensate for DC–offset, which are inherent to the FIR filter structure. IMREG1 is valid for the FIR_REG_1, IMREG2 for FIR_REG_2. In the Table above, IMREG1= IMREG2 = 4. Due to the portioning to 8 bit units the values 4hex and 40hex arise.

Table 4–7: 8 bit FIR–coefficients (decimal integer) for MSP 2410

Mode														
	NICAM		FM–Terrestrial B/G, I	FM – Satellite FIR filtering corresponds to a bandpass filtering with a band width of B = 130 kHz, 180 kHz, 200 kHz, ... 380 kHz										
C (i)	SC/SP	UK	German Dual FM FIR_REG1 and 2	Bandwidth 130 kHz FIR_REG1 *)	Bandwidth 130 kHz FIR_REG2 *)	Bandwidth 180 kHz FIR_REG1	Bandwidth 180 kHz FIR_REG2	Bandwidth 200 kHz FIR_REG1	Bandwidth 200 kHz FIR_REG2	Bandwidth 280 kHz FIR_REG1	Bandwidth 280 kHz FIR_REG2	Bandwidth 380 kHz FIR_REG1	Bandwidth 380 kHz FIR_REG2	Auto–search FIR_REG2
0	–2	2	3	37	73	4	9	1	3	–4	–8	–2	–4	75
1	–8	4	18	27	53	9	18	9	18	–4	–8	–7	–12	15
2	–10	–6	27	32	64	14	28	14	27	2	4	–5	–9	30
3	10	–4	48	60	119	23	47	24	48	19	36	13	23	45
4	50	40	66	51	101	27	55	33	66	41	78	45	79	15
5	86	94	72	65	127	32	64	37	72	57	107	71	126	45



*) The 130 kHz coefficients are based on subcarriers, which are 7 dB below an existent main carrier.

4.2.4. DCO–Increments

For a chosen TV standard a corresponding set of 24–bit increments determining the mixing frequencies of the quadrature mixers, has to be written into the IC. In Table 4–9 some examples of DCO increments are listed. It is necessary to divide them up into low part and high part.

The formula for the calculation of the increments for any chosen IF–Frequency is as follows:

$INCR_{dez} = int(f/fs \cdot 2^{24})$

with: int = integer function
f = IF–Frequency in MHz
f_S = Sampling frequency (18.432 MHz)

Conversion of INCR into hex–format and separation of the 12–bit low and high parts lead to the required increments. (DCO1_HI or _LO for channel 1, DCO2_HI or LO for channel 2).

4.3. Read Registers: Listing and Addresses

The following 8–bit parameters can be read out of the RAM of the MSP 2410; functionally they all belong to the NICAM decoding process; their addresses are listed in Table 4–10.

4.3.1. Read Registers: Functions and Values

C_AD_BITS: NICAM operation mode control bits and A[0–2] of the additional data bits.

Format:

7	6	5	4	3	2	1	0
A[2]	A[1]	A[0]	C4	C3	C2	C1	1
MSB			C_AD_BITS				LSB

Important: Bit[0] must be 1. If this is not the case no correct frame or sequence synchronization have been found yet and the C–Bits are not valid.

The operation mode is coded by C3–C1 as shown in Table 4–8.

Table 4–8: NICAM operation modes

C1	C2	C3	Operation Mode
0	0	0	Stereo sound
0	1	0	Two independent mono channels
1	0	0	One mono signal (S–Bus channel 3)
1	1	0	Data transmission only; no audio

Table 4–9: DCO increments for the MSP 2410; frequency in MHz, increments in Hex

Freq. MHz	DCO_HI	DCO_LO	Freq. MHz	DCO_HI	DCO_LO
4.5	3E8	000			
5.04 5.5 5.58 5.74	460 4C6 4D8 4FC	000 38E 000 0AA	5.76 5.85 5.94	500 514 528	000 000 000
6.0 6.2 6.5 6.552	535 561 5A4 5B0	555 C71 71C 000	6.6 6.65 6.8	5BA 5C5 5E7	AAA C71 1C7
7.02	618	000	7.2	640	000
7.38	668	000	7.56	690	000

Table 4–10: Addresses of read registers

RAM–Position	HEX
c_ad_bits	023
fawct_ist	025
add_bits	038
cib_bits	03E
conc_ct	058
AGC_RMS	007 not of interest for customers

A fifth control bit, C4, is set to 1 only when the FM–mono channel carries the same sound program as the digital stereo signal or the digital mono signal (only the A–channel = S–Bus sample 3 when two digital mono signals are being transmitted).

ADD_BITS: The remaining 8 of the 11 additional data bits that are not defined yet.

Format:

7	6	5	4	3	2	1	0
A[10]	A[9]	A[8]	A[7]	A[6]	A[5]	A[4]	A[3]
MSB			ADD_BITS				LSB

CIB_BITS: cib bits 1 and 2 (see NICAM 728 specifications)

Format:

7	6	5	4	3	2	1	0
x	x	x	x	x	x	CIB1	CIB2
MSB			CIB_BITS				LSB

FAWCT_IST : The contents of this register give information on the actual position of the FAW–counter. For optimum NICAM performance, the value should be identical with or little below the value of 'FAW_SOLL'. If it reaches 0 the FP–software mutes and stops the NICAM–decoding automatically by searching for FAW synchronization once more.

CONC_CT : The contents of this register contain the actual number of bit errors of the previous 728 bit data frame. It may happen that in spite of acceptable FAWCT_IST the bit error rate result is too high for appropriate sound performance. In this case the CCU can switch to the analog FM–sound assumed to have the same program (Control bit C4).

4.4. Communication Rules CCU/MSP 2410

There are 2 general rules for the syntax: The first transmitted 8 bits are always an IM–Bus register address. The second 8 or 16 bits can be a RAM–address for the FP or a data value:

– a. 8 bit Address for IM–Bus register
  b. 8 or 16 bit data, which can be a RAM–address or a data value
– Every data or address word has to be transmitted with the LSB always first.

In the following the name of an IM–Bus register in brackets { } means that the corresponding address will be sent to the MSP 2410 IM–Bus interface.

Example: {WRITE_ADR} means the address A0 (see 2.2.1.).

To write or to read a value into or out of the (already addressed) DATA register, the value has to be sent immediately after addressing the DATA register.

Example: Value means:

Read 'DATA' register in case of {READ_ADR} or

write into 'DATA' in case of {WRITE_ADR}

Before starting any new IM–Bus activity with the MSP 2410, the CCU has to check whether the MSP 2410 has terminated any previous data transmission by means of the Busy Bit (=bit[2] of 'STATUS'):

0a. 0b.	{STATUS} Status	[7:0] [7:0]	Address of STATUS register Read STATUS register
	Busy Bit = 0 ?		
	yes → new IM–Bus activity no → 0a.		

4.4.1. Writing an 8–Bit Data Word into the MSP 2410

0a. 0b.	{STATUS} Status	[7:0] [7:0]	Address of STATUS register Read STATUS register
	Busy Bit = 0?		
	yes → 1a. no → 0a.		
1a. 1b. 2a. 2b.	{WRITE_ADR} Adr {DATA} Value	[7.0] [15:0] [7:0] [7:0]	Address of WRITE_ADR register Desired RAM–Address (see 4.1.) Address of DATA register Write Value into DATA register

4.4.2. Writing a 12–Bit Data Word into the MSP 2410

0a. 0b.	{STATUS} Status	[7:0] [7:0]	Address of STATUS register Read STATUS register
	Busy Bit = 0?		
	yes → 1a. no → 0a.		
1a. 1b. 2a. 2b. 3a. 3b.	{EXT_ADR} Value {WRITE_ADR} Adr {DATA} Value	[7:0] [15:0] [7:0] [15:0] [7:0] [7:0]	Address of EXT_ADR register 12 bit value (LSB bound; 4 MSBs = 0) Address of WRITE_ADR register Desired RAM–Address (see 4.1.) Address of DATA register Write dummy value into DATA register

4.4.3. Reading 8–Bit DATA out of the MSP 2410

0a. 0b.	{STATUS} Status	[7:0] [7:0]	
	Busy Bit = 0?		
	yes → 1a. no → 0a.		
1a. 1b.	{READ_ADR} ADR	[7.0] [15:0]	Address of READ_ADR register RAM–Address to read
2a. 2b.	{STATUS} STATUS	[7:0] [7:0]	FP writes desired value into DATA
	Busy Bit = 0?		
	yes → 3a. no → 2a.		
3a. 3b.	{DATA} Value	[7:0] [7:0]	Address of DATA register Read DATA register

4.4.4. Address for Defined FP–Program Jumps

Via the IM–Bus the FP–Software can be forced to continue at a label (JUMP_ADR) whose address was determined by the CCU. The following address format must be chosen:

Register	**MSB**						**Bit**									**LSB**
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
JUMP_ADR	0	0	0	0	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

A11–A0 : Complete address of the desired FP–routine, which is automatically even (LSB=!0).

4.4.5. IM–Bus Syntax for Starting a Defined FP routine

0a. 0b.	{STATUS} Status	[7:0] [7:0]	Address of STATUS register Read STATUS register
	Busy Bit = 0?		
	yes → 1a. no → 0a.		
1a. 1b. 2a. 2b.	{WRITE_ADR} Adr {DATA} Value	[7:0] [15:0] [7:0] [7:0]	 Jump Address (s. above) 8 Bit Data (Dummy)

The following routines can be started by means of program jumps (Hex–value is JUMP_ADR A11–A0).

Routine	Address	Function
0. RESET_SCHEDULER	0000 HEX	Resets FP–Program counter to 0000 (not relevant for user)
1. LOAD_REG_0	0056 HEX	After switch on or changing the TV system (B/G to I, I to B/G) all write–parameters have to be transmitted via IM–Bus into the MSP 2410. Then 'Load_REG_0' writes them into the corresponding registers. FM–processing starts.
2. LOAD_REG_1	0060 HEX	In the case of a TV–Standard change in MSP channel 1, only new channel 1 parameters have to be transmitted into the IC via IM–Bus. These are: FIR_REG_1, MODE_REG, DCO1_LO/HI.
3. SEARCH_SCHEDULER	0078 HEX	To start the NICAM–processing, this address has to be transmitted into the FP.
4. RAM_TEST	0792 HEX	Check of the FP ALU

4.5. Sequences to Transmit Parameters and Start of Processing

After having been switched on, the MSP 2410 has to be initialized by transmitting the parameters according to the LOAD_SEQ_0 of Table 4–11. After that all parameters are stored in the RAM of the FP. To make the FP load them into the corresponding internal registers, the load routine LOAD_REG_0 must be activated (4.4.4).

For NICAM operation the following steps listed in 'NICAM_START, _READ and _Check' in Table 4–11 must be taken.

For FM–stereo operation no more steps concerning the MSP 2410 must be taken. The evaluation of the identification signal must be performed as described in the ACP 2371 data sheet. For positive identification check, the AMU 2481 VS sound channels have to be switched corresponding to the detected operation mode.

NOTE: Before the CCU gets the results of the NICAM or FM–identification signal check, the AMU 2481 VS has to be switched to the basic FM–mono channel, which is available on Sample 1 and 2 of the S–Bus. For detailed information concerning AMU switching please refer to the AMU 2481 VS data sheet.

Table 4–11: Sequences to initialize and start the MSP 2410

LOAD_SEQ_0: General Initialization, followed by LOAD_REG_0		
Write into MSP 2410:		
0. AD_CV	(see section 4.1.)	**In the case of "NICAM only" operation, the steps 9. and 10. can be skipped**
1. Audio_PLL	(LSB of 8 bit)	
2. FAWCT_SOLL	(8 bit; only for NICAM mode)	
3. FAW_ER_TOL	(8 bit; only for NICAM mode)	
4. FIR_REG_1	(6 · 8 bit; see 4.2.2.)	
5. FIR_REG_2	(9 · 8 bit; see 4.2.2.)	
6. MODE_REG	(12 bit; see 4.2.1.)	
7. DCO1_LO	(12 bit; see 4.2.3.)	
8. DCO1_HI		
9. DCO2_LO		
10. DCO2_HI		
11. JUMP LOAD_REG_0	(see 4.4.4.); FM–processing starts	
NICAM_START: Start of the NICAM Software		
Write into MSP 2410:		
1. JUMP SEARCH_SCHEDULER	(see 4.4.4.)	
2. Wait at least 0.5 s		

Table 4–11, continued

NICAM_READ: Read NICAM specific information
Read out of MSP 2410: 1. FAWCT_IST (see 4.3.) 2. C_AD_BITS (see 4.3.) 3. CONC_CT (see 4.3.)
NICAM_CHECK: CCU checks for presence, operation mode and quality of NICAM signal
1. Evaluation of parameters in the CCU 2. If necessary, switch the AMU 2481 VS sound channels
FM_IDENT_CHECK: See ACP data sheet: Decoding of the identification signal
1. Evaluation of ACPs IDLEV in the CCU 2. If necessary, switch the AMU 2481 VS sound channels
LOAD_SEQ_1: Reinitialization of Channel 1 without affecting Channel 2, followed by LOAD_REG_1
Write into MSP 2410: 1. FIR_REG_1 (6 · 8 bit; see 4.2.2.) 2. MODE_REG (12 bit; see 4.2.1.) 3. DCO1_LO (12 bit; see 4.2.3.) 4. DCO1_HI 5. JUMP LOAD_REG_1 (see 4.4.4.)

4.6. Software Proposals for Multistandard TV–Sets

To familiarize the reader with the programming scheme of the MSP 2410, two examples in the shape of flow diagrams are shown in the following sections.

4.6.1. Multistandard Including System B/G with NICAM/FM–Mono only

Fig. 4–1shows a flow diagram for the CCU software, applied for the MSP 2410 in a TV set, which facilitates NICAM and FM–mono sound. For the instructions please refer to Table 4–11.

If the program is changed, resulting in another program within the Scandinavian System B/G no parameters of the MSP 2410 have to be modified. To facilitate the check for NICAM the CCU has only to continue at the 'NICAM_START' instruction. During the 'NICAM_CHECK' the AMU must switch to the FM–mono sound of course.

4.6.2. Multistandard Including System I with NICAM/FM–Mono only

This case is identical to the one above. The only difference consists in selecting the UK parameters for DCO1_LO/HI, DCO2_LO/HI and FIR_REG_1.

4.6.3. Multistandard Including System B/G with NICAM/FM–Mono and German DUAL FM

Fig. 4–2 shows a flow diagram for the CCU software, applied for the MSP 2410 in a TV set, which facilitates all standards according to System B/G. For the instructions used in the diagram please refer to Table 4–11.

After having switched on the TV–set and having initialized the MSP 2410 (LOAD_SEQ_0), FM–mono sound is available. Therefore the AMU should switch its S–Bus output to the corresponding S–Bus inputs (Sample 1,2). Also bit 1 of K33 has to be set to 1 (see AMU 2481 VS data sheet).

Fig. 4–2 shows that to check for any stereo or bilingual audio information in channel 1, its parameter should be loaded with NICAM and FM2 parameters alternately (LOAD_SEQ_1). In the case of success the AMU has to switch to the desired audio mode.

4.6.4. Satellite Mode

Fig. 4–3 shows the simple flow diagram to be used for the MSP2410 in a satellite receiver. For FM–mono operation the corresponding FM carrier should preferably be processed at the MSP–channel 2, whereas the AMU_VS has to distribute the mono signal to the left and right outputs.

4.6.5. Automatic Search Function for FM–Carrier Detection

The AM demodulation ability of the MSP 2410 offers the possibility to calculate the “field strength” of the momentarily selected FM carrier, which is transmitted via S–Bus to the AMU 2481_VS. Here it can be read out by the CCU. In SAT receivers this feature can be used to realize an automatic FM carrier search.

Therefore the MSP has to be switched to AM–mode (Bit 8 of MODE_REG). The sound–IF frequency range must now be “scanned” in the MSP–channel 2 by means of the programmable quadrature mixer with an appropriate incremental frequency (i.e. 10 kHz).

After each incrementation there is a field strength value available at the AMU_VS register 63 (RMS A), which must be examined for relative maxima by the CCU. This results in either continuing search or switching the MSP back to FM demodulation mode.

During the search process the FIR_REG_2 must be loaded with the coefficient set “AUTOSEARCH”, which enables small bandwidth resulting in appropriate field strength characteristics. The absolute field strength value also gives information on whether a main FM carrier or a subcarrier was detected, and as a practical consequence the FM bandwidth (FIR_REG_1/2) and the deemphasis (50 µs or adaptive) can be switched automatically. For a detailed description of the automatic search function please refer to the corresponding CLIMB program.

4.6.6. Automatic Standard Detection

The AM demodulation ability of the MSP 2410 enables also a simple method to decide between standard B/G (FM–carrier at 5.5 MHz) and standard I (FM–carrier at 6.0 MHz). It is achieved by tuning the MSP in the AM–mode to the two discrete frequencies and evaluating the field strength values available at the AMU_VS register 63 (RMS A) in the CCU.

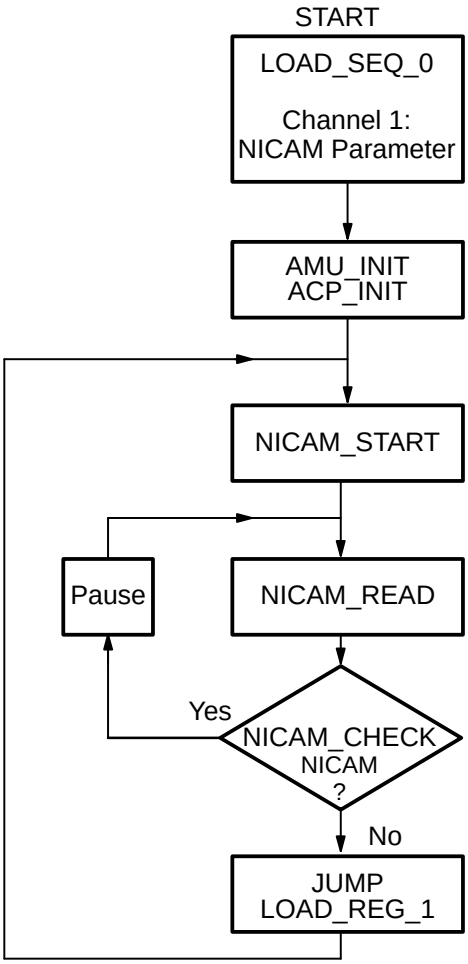


Fig. 4–1: CCU software flow diagram: Standard B/G/I NICAM/FM mono only
Note: AMU should switch its output channels basically to FM_Mono Output of MSP 2410

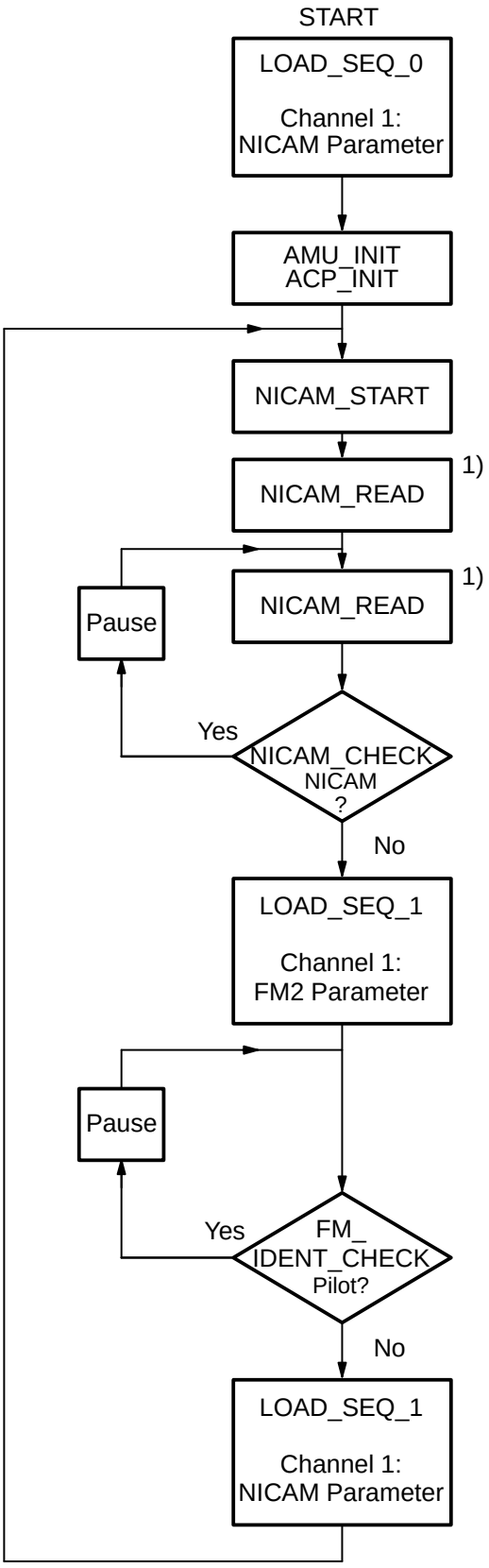


Fig. 4–2: CCU software flow diagram: Standard B/G with NICAM or FM stereo

Note: AMU should switch its output channels basically to FM_Mono Output of MSP 2410

1) The first READ could result in incorrect values

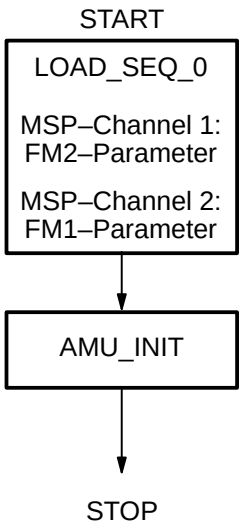


Fig. 4–3: CCU software flow diagram: SAT–mode

5. Specifications

5.1. Outline Dimensions

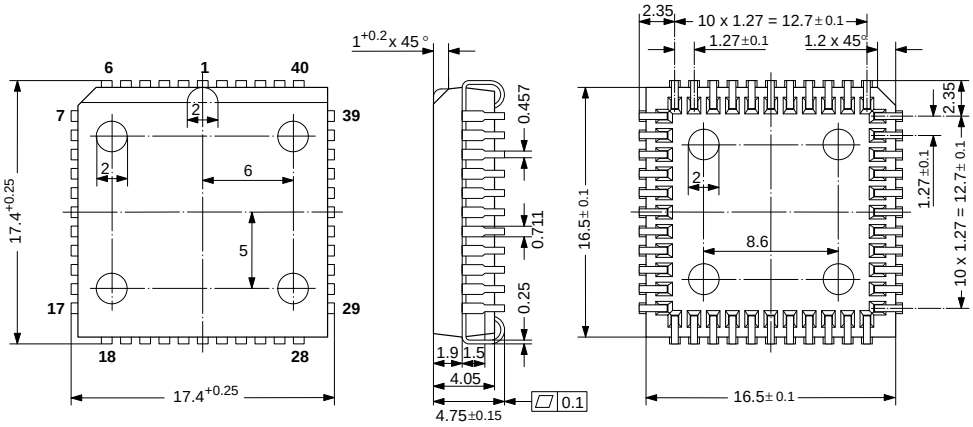


Fig. 5–1: MSP 2410 (S) in 44–pin PLCC package
Weight approx. 2.5 g, Dimensions in mm

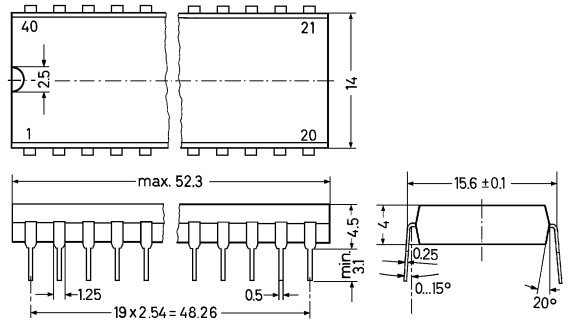


Fig. 5–2: MSP 2410 (S) in 40–pin DIL package
Weight approx. 6 g, Dimensions in mm

5.2. Pin Connections and Descriptions (Fig. 5–3) and (Fig. 5–4)

n.a. = not available; * = if not used

Pin No. PLCC	Pin No. DIL	Input: I, Output: O	Pin Name	Short Description
1	40	I	IMIDENT	IM–Bus Ident
2	39	I/O	IMDAT	IM–Bus Data
3	38	I	IMCLOCK	IM–Bus Clock
4	37	I	CWDATA/SCANIN	Pay–TV Data/Test input (* connect to ground)
5	n.a.	I	FRAME/SCAN-OUT	Frame 1 kHz/Test output (* leave vacant)
6	36	I	TESTIO	for test only (* connect to ground)
7	35	I	CWCLCK/LTIOSC	Pay–TV Clock/Test input (* connect to ground)

Pin Connections and Descriptions, continued

Pin No. PLCC	Pin No. DIL	Input: I, Output: O	Pin Name	Short Description
8	n.a.	I	ROMTEST	for test only (* connect to ground)
9	34	O	RDSOUT	for test only (* leave vacant)
10	33	I	PORQ	Power On Reset (active low)
11	32	O	SIDENT	S–Bus Ident
12	31	O	SCLOCK	S–Bus Clock
13	30	O	SDATA	S–Bus Data Out
14	29		GND	Ground (digital)
15	28		VSUP	Supply voltage (digital)
16	27	O	AUDIOCLOCK	Main Clock for AMU, APU, ADC or ACP
17	26	O	VADCLOCK	Clock for external A/D Converter (* leave vacant)
18	25	O	PWMFM2	FM2 channel for FM–identification; to be connected to pin 8 via the bandpass of ADC 2311 E, or pin 19 of ACP If bit [7] of Mode_REG is 0, PWM FM2 = 0 (low)
19	24	I/O	NBUSDAT	NICAM_728 serial I/O (* leave vacant)
20	23	I/O	NBUSCLOCK	Clock of digital NICAM bit stream (* leave vacant)
21	22	O	DIGOUT0	Digit. Output LSB (Test, connect to ground if not used)
22	21	O	DIGOUT1	Digit. Output LSB (Test, connect to ground if not used)
23	20	O	DIGOUT2	Digit. Output LSB (Test, connect to ground if not used)
24	19	O	DIGOUT3	Digit. Output LSB (Test, connect to ground if not used)
25	18	O	DIGOUT4	Digit. Output LSB (Test, connect to ground if not used)
26	17	O	DIGOUT5	Digit. Output LSB (Test, connect to ground if not used)
27	16	O	DIGOUT6	Digit. Output LSB (Test, connect to ground if not used)
28	n.a.	O	DIGOUT7	Digit. Outp. MSB (Test, connect to ground if not used)
29	15	I	DIGIN7	Digital Input MSB (from ext. A/D–converter)(* connect to ground when using internal A/D–converter)
30	14	I	DIGIN6	(from ext. A/D–converter)(* connect to ground when using internal A/D–converter)
31	13	I	DIGIN5	(from ext. A/D–converter)(* connect to ground when using internal A/D–converter)
32	12	I	DIGIN4	(from ext. A/D–converter)(* connect to ground when using internal A/D–converter)
33	13	I	DIGIN3	(from ext. A/D–converter)(* connect to ground when using internal A/D–converter)

Pin Connections and Descriptions, continued

Pin No. PLCC	Pin No. DIL	Input: I, Output: O	Pin Name	Short Description
34	n.a.	I	DIGIN0	Digital Input LSB (* connect to ground when using internal A/D–converter)
35	10	I	EXTCLOCK	Input for ext. clock (D2–MAC) to be passed through the MSP 2410
36	9		XTAL1	Crystal Input (18.432 MHz)
37	8		XTAL2	Crystal Output (18.432 MHz)
38	7	I	DIGIN2	(from ext. A/D–converter)(* connect to ground when using internal A/D–converter)
39	6		VSUPANALOG	A/D–converter: Supply Voltage (5 V)
40	5		GNDANALOG	A/D–converter: Ground
41	4	I	ANALOGIN1 +	Sound–IF input from first audio source
42	3		ANALOGIN –	Common Ground of Sound–IF sources 1 and 2
43	2	I	ANALOGIN 2+	Sound IF input from second audio source. Test mode: DIGIN 1
44	1		VREFTOP	A/D–converter: Top Reference Voltage

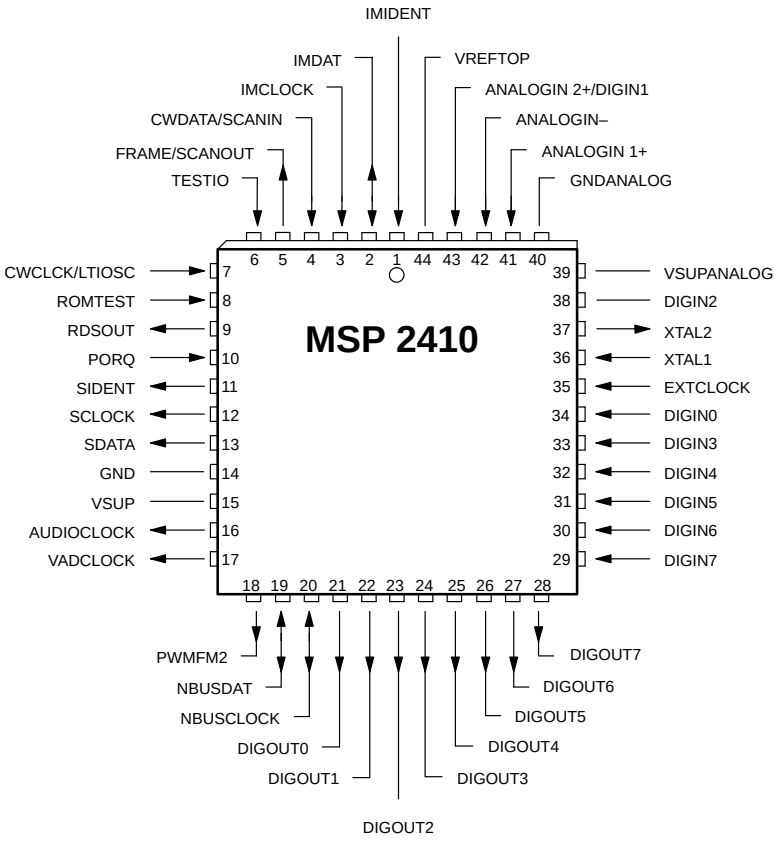


Fig. 5–3: Pinning of the MSP 2410 in 44–pin PLCC package (top view)

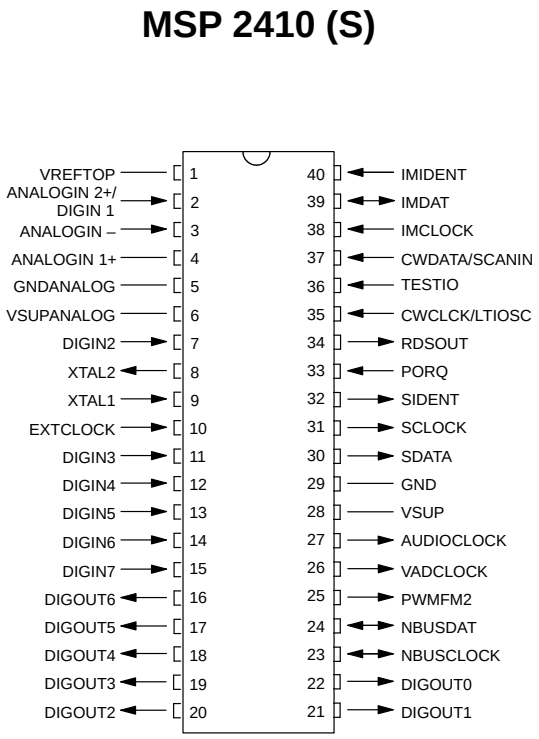


Fig. 5–4: Pinning of the MSP 2410 (S) in 40–pin DIL package (top view)

5.3. Pin Circuits (pin numbers for 44–pin PLCC package)

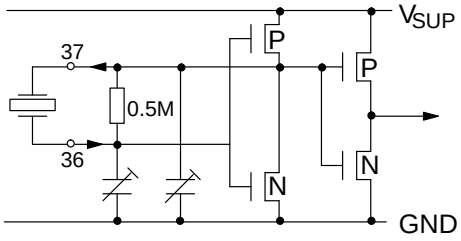


Fig. 5–5:
Pins 36 and 37

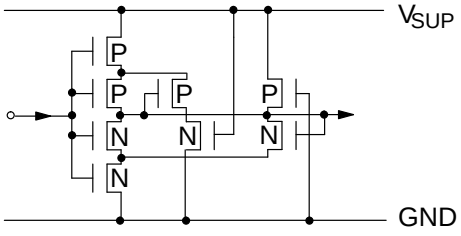


Fig. 5–6:
Input Pin 10

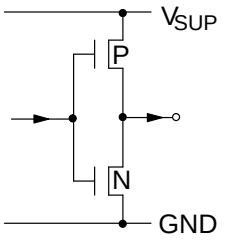


Fig. 5–7:
Output Pins 5, 17, 18

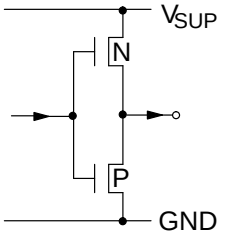


Fig. 5–8:
Output Pin 16

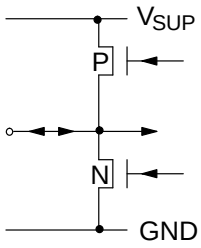


Fig. 5–9:
Input/Output Pins 19 and 20

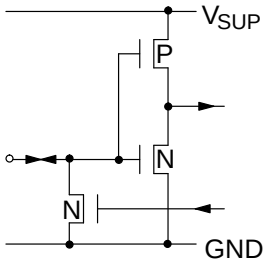


Fig. 5–10:
Input/Output Pin 2

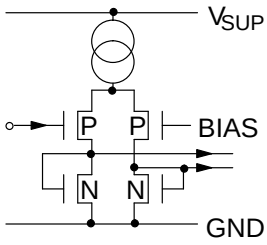


Fig. 5–11:
Input Pin 35

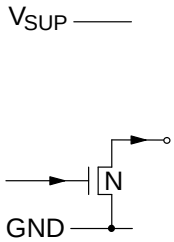


Fig. 5–12:
Output Pins 11, 12, 13

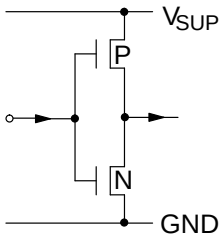


Fig. 5–13:
Input Pins 1, 3, 4, 7, 43

Note: Circuits for test pins not given.

5.4. Electrical Characteristics (pin numbers for 44–pin PLCC package)

5.4.1. Absolute Maximum Ratings

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit
T_A	Ambient Operating Temperature	–	0	–	80	°C
T_S	Storage Temperature	–	–40	–	125	°C
V_{SUP}	Supply Voltage, (analog, digital)	15, 39	–	–	6	V
V_I	Input Voltage all Inputs	–	–0.3 V	–	V_{SUP}	–
V_O	Input Voltage all Outputs	–	–0.3 V	–	V_{SUP}	–
I_O	Latch–up Input Current	all pins	– 50	–	50	mA

5.4.2. Recommended Operating Conditions at T_A = 0 to 65 °C

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit
V_{SUP}	Supply Voltage	15, 39	4.75	5.0	5.25	V
V_{REIL}	Reset Low Voltage	10	–	–	0.8	V
V_{REIH}	Reset High Voltage	10	2.4	–	–	V
t_{REIL}	Reset Low Time	10	5	–	–	µs
V_{DIGIL}	Digital Input Low Voltage	1, 2, 3, 4, 7, 19, 20	–	–	0.8	V
V_{DIGIH}	Digital Input High Voltage		2.4	–	–	V
$V_{EXTCLIL}$	EXTCLOCK Input Low Voltage	35	–	–	1.5	V
$V_{EXTCLIH}$	EXTCLOCK Input High Voltage	35	3.5	–	–	V
t_{EXTLH}	EXTCLOCK Transition Time Low $\rightarrow$ High	35	–	–	10	ns
t_{EXTHL}	EXTCLOCK Transition Time High $\rightarrow$ Low	35	–	–	10	ns
F_{EXT}	EXTCLOCK Frequency	35	–	18.432	–	MHz
f_{IM}	IM Bus Frequency	3	5	–	1000	kHz
t_{IM1}	Clock Input Delay Time After IM Bus Ident Input	3	0	–	–	–
t_{IM2}	Clock Input Low Pulse Time	3	500	–	–	ns
t_{IM3}	Clock Input High Pulse Time	3	500	–	–	ns
t_{IM4}	Clock Input Setup Time before Ident High	3	0	–	–	–

Recommended Operating Conditions, continued

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit
t_{IM5}	Clock Input Setup Time after Ident High	3	250	–	–	ns
t_{IM6}	Clock Input Setup Time before Ident End Pulse	3	1	–	–	µs
t_{IM7}	Data Input Delay Time after Clock	2	0	–	–	–
t_{IM8}	Data Input Setup Time before Clock	2	0	–	–	–
t_{IM9}	Data Input Hold Time after Clock	2	0	–	–	–
t_{IM10}	Ident End–Pulse Low Time	1	1	–	–	µs
Crystal Recommendations						
f_P	Parallel Resonance Frequency at 10 pF Load Capacitance	–	–	18.432	–	MHz
f_{TOL}	Accuracy of Adjustment	–	–30	–	30	ppm
D_{TEM}	Frequency Deviation versus Temperature	–	–30	–	30	ppm
R_R	Series Resistance	–	–	–	25	Ohm
C_0	Shunt (Parallel) Capacitance	–	–	–	7	pF
C_1	Motional (Dynamic) Capacitance	–	15	–	–	fF
Load Capacitance						
C_{LI}	Internal (Open Loop: NICAM not active)	–	–	5	–	pF
C_{LE}	External (Incl. Capacitance of Socket) per pin	36, 37	1.5	5	10	pF
F_{CL}	Required Open Loop Clock Frequency (=NICAM not active)	16,17	18.431	18.432	18.433	MHz
Recommendations for Analog Sound IF Input Signal						
V_{IF}	Analog Input Range (Complete Sound IF, 0 – 9 MHz)	41, 43	0.14	0.8	3	Vpp
R_{FMNI}	Ratio: NICAM Carrier/FM Carrier (unmod. carriers) BG: I:	41, 43	 –17 –20	 –7 –10	 0 0	 dB dB

Recommended Operating Conditions, continued

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit
R_{FM}	Ratio: FM-Main/FM-Sub Satellite	41, 43		7		dB
$R_{FM1/FM2}$	Ratio: FM1/FM2 German FM-System	41, 43		7		dB
R_{FC}	Ratio: Main FM Carrier/ Color Carrier	41, 43	15	–	–	dB
R_{FV}	Ratio: Main FM Carrier/ Luma Components	41, 43	15	–	–	dB
PR_{IF}	Passband Ripple	41, 43	–	–	±2 dB	dB
SUP_{HF}	Suppression of Spectrum Above 9.0 MHz	41, 43	15		–	dB
FM_{MAX}	Maximum FM–Deviation	41, 43		190	–	kHz

5.4.3. Characteristics at T_A = 0 to 65 °C, V_{SUP} = 4.75 to 5.25 V, f_{CL} = 18.432 MHz; load capacity max. 30 pF.

Symbol	Parameter	Pin. No.	Min.	Typ.	Max.	Unit	Test Conditions
I_{SDIG}	Supply Current Digital + Analog	15, 43	–	120	150	mA	f_{CL} = 18.432 MHz
V_{IMOL}	IM Bus Data Output Low Voltage	2	–	–	0.4	V	I_{IMOL} = 5 mA
I_{IMOL}	IM Bus Data High Current	2	–	–	10	µA	
V_{VADOL}	VADCLOCK Output Low Voltage	17	–	–	0.4	V	I_{VADO} = 9.5 mA
V_{VADOH}	VADCLOCK Output High Voltage	17	4.0	–	–	V	$-I_{VADO}$ = 9.5 mA
f_{VAD}	VADCLOCK Frequency	17	–	18.432	–	MHz	in NICAM mode
t_{VAD}	Transition Time	17	–	–	10	ns	Load = 30 pF
V_{APUOL}	Audio Clock Output AC Voltage	16	0.8	–	2.5	V_{pp}	
V_{APUOH}	Audio Clock Output DC Voltage	16	1.5	–	3.5	V	
f_{APU}	Audio Clock Frequency	16	–	18.432	–	MHz	in NICAM mode
t_{APU}	Transition Time	16	–	–	15	ns	Load = 30 pF
V_{DPPOL}	Digital Output Low Voltage Push-Pull	5, 19, 20	–	–	0.4	V	I_{VDPPO} = 3 mA

Characteristics, continued

Symbol	Parameter	Pin. No.	Min.	Typ.	Max.	Unit	Test Conditions
V_{DPPOH}	Digital Output High Voltage Push-Pull	5, 19, 20	4.0	–	–	V	$-I_{VDPDO}$ = 3 mA
V_{SOL}	S-Bus Output Low Voltage	11, 12, 13	–	–	0.4	V	I_{SOL} = 8 mA
I_{SOH}	S-Bus Output High Current	11, 12, 13	–	–	10	µA	V_{SOH} = 5 V
t_{SOT}	S-Bus High to Low Transition Time at Load = 30 pF	11, 12, 13	–	–	10	ns	
f_S	S-Bus Clock Output Frequency	12	–	4.608	–	MHz	
$t_{S1/S2}$	S-Bus Clock Output High/Low Ratio	12	0.9	1.0	1.1	–	
t_{S3}	S-Bus Clock Setup Time before Ident End Pulse	11, 12	200	220	–	ns	
t_{S4}	S-Bus Data Setup Time before Clock	12, 13	100	–	–	ns	
t_{S5}	S-Bus Data Hold Time after Clock	12, 13	110	–	–	ns	
t_{S6}	S-Bus Ident End Pulse Low Time	11	200	220	–	ns	
V_{PWMOH}	PWM Output High Voltage	18	4.0	–	–	V	$-I_{PWMOH}$ = 1 mA
V_{PWMOL}	PWM Output Low Voltage	18	–	–	0.8	V	I_{PWMOH} = 1 mA
S/N_{FM}	FM: S/N via AMU 2481 VS	13	70	–	–	dB	1 FM-carrier, 50 µs, 1 kHz 40 kHz deviation; RMS, un-weighted 0 to 15 kHz; full input range
FM_{OUT}	Digital FM-Level on S-Bus FM Deviation: 50 kHz 75 kHz 150 kHz 192 kHz	–	–	 –16.5 –12.5 –6.5 –4.5	–	dB FDS (Full Digital Scale)	Values include FM Block (CFI: –1.5 dB) and CFII (AMU_VS: –3dB)
THD_{FM}	Total Harmonic Distortions + Noise via AMU 2481 VS	13	–	–	0.3	%	1 FM–carrier, 1 kHz, 50 µs; 40 kHz deviation; full input range
BER_{NI}	NICAM: Bit Error Rate	–	–	–	10^{-7}	/s	FM+NICAM, norm conditions
R_{IFIN}	Input Impedance	41, 43	–	2	–	kOhm	
$DC_{VREFTOP}$	DC Output Voltage at VREFTOP	44	–	2.67	–	V	$V_{SUPANALOG}$ = 5V
$DC_{ANA-LOGIN1+}$	DC Output at ANALOGIN1+	41	–	1.5	–	V	$V_{SUPANALOG}$ = 5V
$DC_{ANALOGIN-}$	DC Output Voltage at VREFTOP	42	–	1.5	–	V	$V_{SUPANALOG}$ = 5V

6. Application Circuit

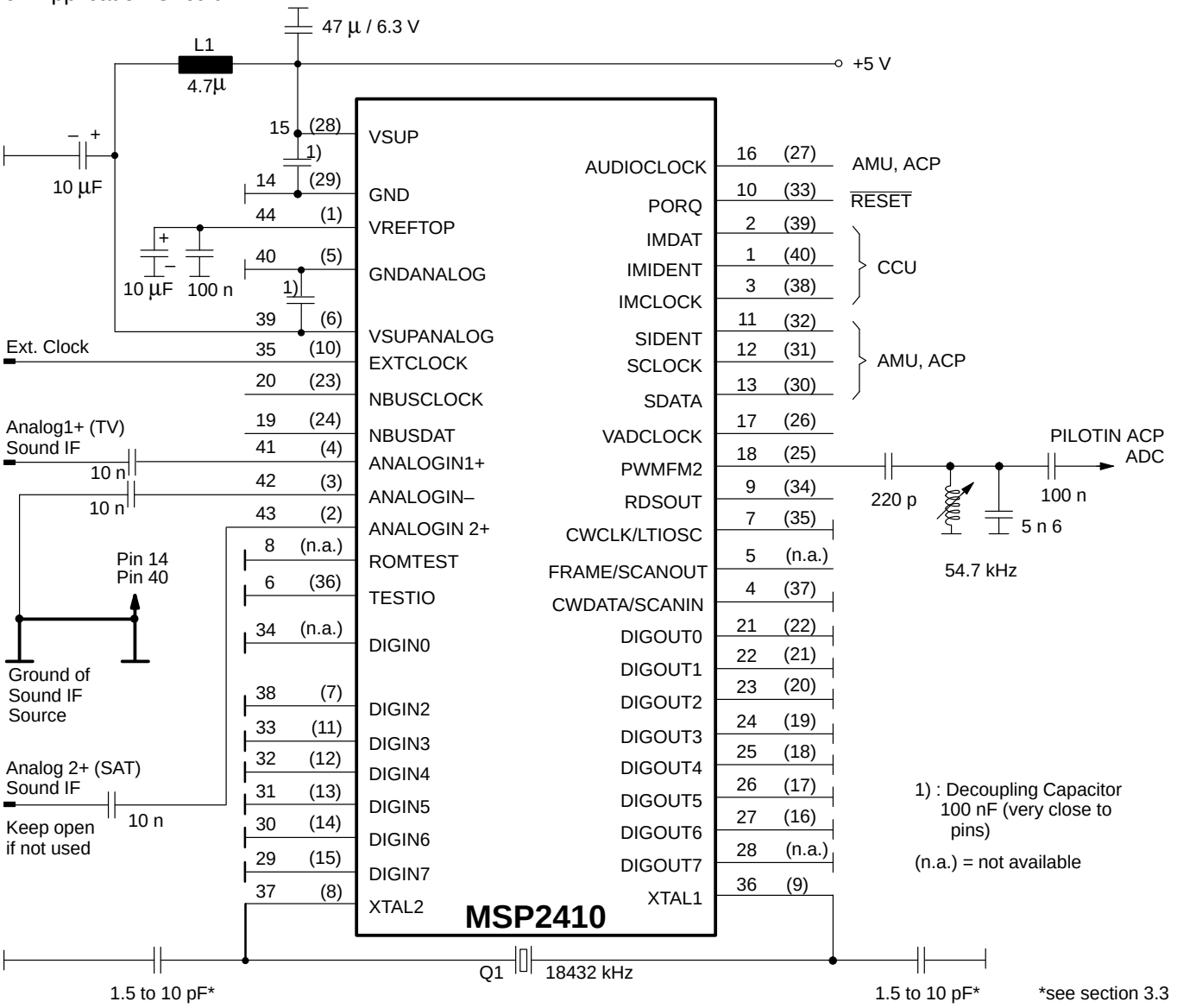
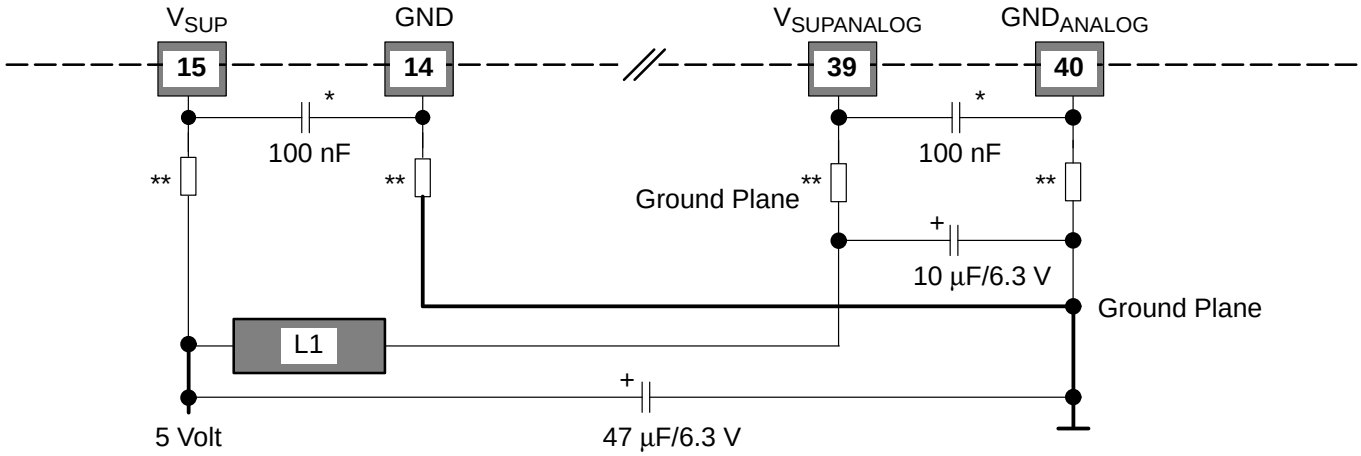


Fig. 6–1: MSP 2410 application circuit

Note: The numbers in brackets refer to the DIL version pinning of the MSP 2410 (S).



*** decoupling capacitors very close to pins (< 5 mm)** **** unavoidable narrow V_{SUP} and ground lines**

Fig. 6–2: Perfect grounding layout

7. Index

W

8. Data Sheet History

– page 26: Figs. 5–1 and 5–2 changed

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End of Data Sheet

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