DESCRIPTION

The MP1006 is a high performance off-line CCFL/EEFL controller designed for powering the Cold Cathode Fluorescent Lamp (CCFL) and External Electrode Fluorescent Lamp (EEFL), especially for multi-lamp Liquid Crystal Display (LCD) backlighting applications.

The MP1006 utilizes fixed operating frequency PWM control to the inverter. It outputs two 180 degree phase shifted driving signals for various external power stages. Its enhanced 9V gate driver provides adequate driving capability for the external MOSFETs. It is able to directly drive the external gate driving transformer. The inverter converts unregulated DC voltage to a nearly sinusoidal lamp voltage to power up CCFL or EEFL lamps.

The MP1006 implements burst mode dimming to the lamp. Burst mode dimming is controlled with either an external DC voltage or PWM signal.

The Built-in fault management features include open lamp regulation and protection, short circuit protection and over temperature protection. The protection interface is flexible for various setups and is easy to use.

The MP1006 is available in a 16-pin SOIC package.

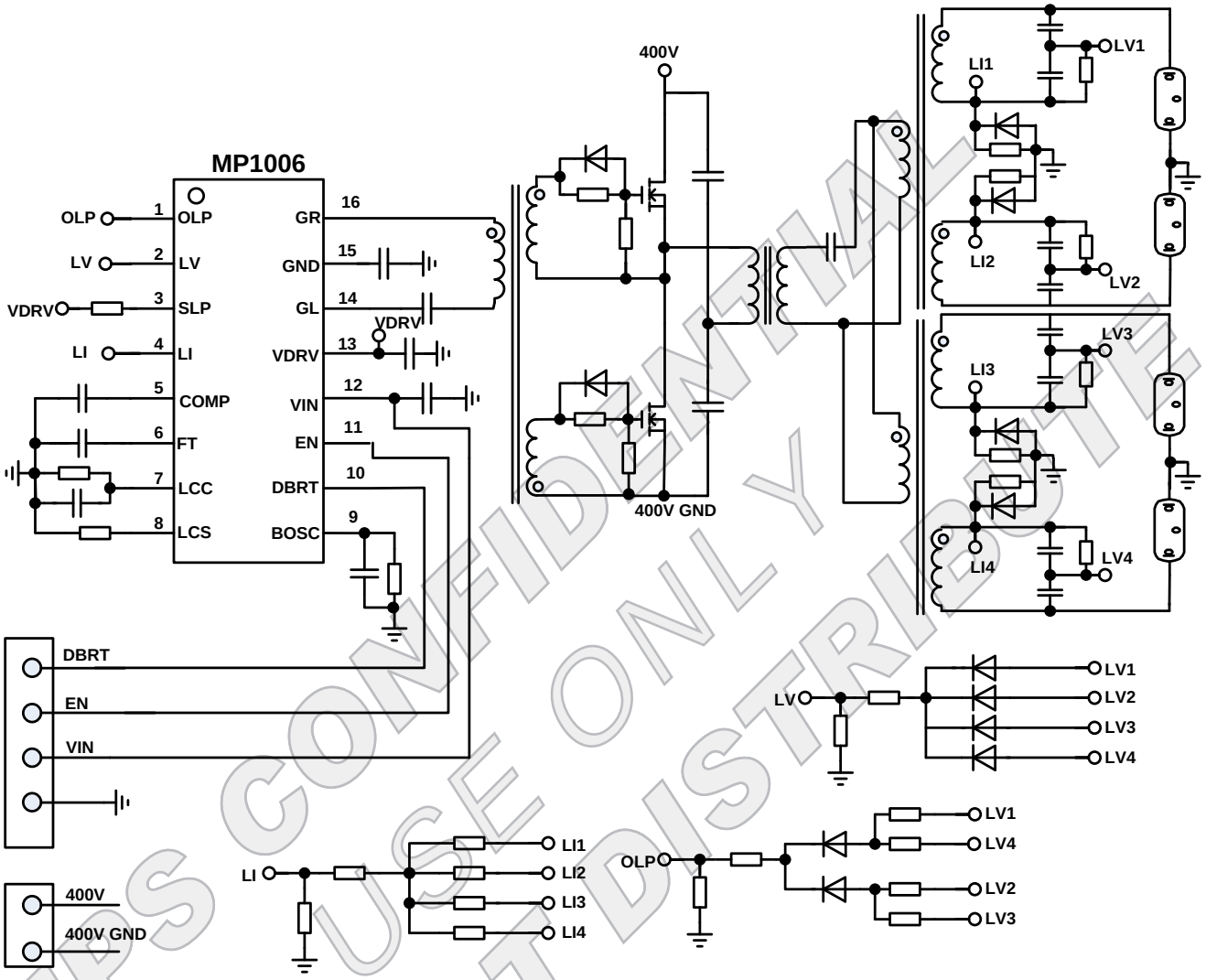
FEATURES

- 9V Enhanced Gate Driver, Can Directly Drive the Gate Driving Transformer
- Programmable Fixed Operating Frequency
- Input Voltage Range from 9V to 30V
- Lamp Current and Voltage Regulation
- Burst Mode Dimming Control
- Integrated Burst Mode Oscillator and Modulator
- Soft-On and Soft-Off Burst Envelope
- Smart Fault Protection Interface
- Built-in fault management
- Dual Mode Fault Timer
- Programmable Striking Frequency, Striking Time and Burst Dimming Frequency
- Unique Short Circuit Current Limitation
- Available in SOIC 16 Package

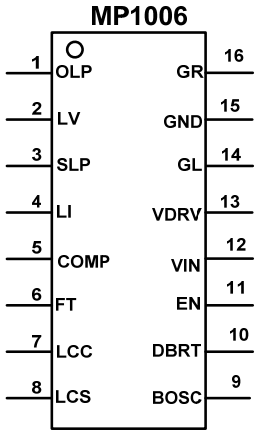
APPLICATIONS

- LCD TV and LCD Monitor in Off-line System
- Flat Panel Video Displays
- Off Line Inverter for CCFL/EEFL driver

SIMPLIFIED TYPICAL APPLICATION



PACKAGE REFERENCE



Part Number*	Package
MP1006ES	SOIC16
Temperature	**Top Marking**
–20°C to +85°C	MP1006ES

* For Tape & Reel, add suffix –Z (eg. MP1006ES–Z)
For RoHS Compliant Packaging, add suffix –LF (eg. MP1006ES–LF–Z)

ABSOLUTE MAXIMUM RATINGS (1)

Input Voltage V_{IN} 35V
GL, GR ..... -0.3V to 10.7V
Logic Inputs, LV, OLP .....–0.3V to +6.5V
LI, SLP .....–5.8V to +5.8V
Junction Temperature ..... 150°C
Lead Temperature (Solder)..... 260°C
Operating Frequency 150KHz
Storage Temperature..... –55°C to +150°C

Recommended Operating Conditions (2)

Input Voltage V_{IN} .....9V to 30V
Operating Frequency .....20KHz to 100KHz
Operating Frequency (Typical) 50KHz
Operating Temperature..... –20°C to + 85°C

Thermal Resistance (3)

	θ_{JA}	θ_{JC}
SOIC16	80	30 ... °C/W

Notes:
1) Exceeding these ratings may damage the device.
2) The device is not guaranteed to function outside of its operating conditions.
3) Measured on JESD51-7, 4-layer PCB

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_A = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Gate driver GL, GR						
Gate Pull-Down	R_{GD}			2		Ω
Gate Pull-Up	R_{GU}			4		Ω
Output Source Current	I_{SOURCE}			1		A
Output Sink Current	I_{SINK}			2		A
Maximum Duty Cycle	D_{MAX}			46%		
EN						
EN Turn On Threshold	V_{EN-ON}		2			V
EN Turn Off Threshold	V_{EN-OFF}				1	V
Internal Pull-down Resistor	R_{EN-IN}			60		kΩ
Brightness Control Range						
DBRT Full Scale	V_{DBRT}	DC burst dimming	1.1	1.2	1.3	V
DBRT Logic Input Threshold	$V_{TH-DBRT}$	PWM dimming	1.6	1.9	2.2	V
DBRT Logic Input Hysteresis	$V_{TH-DBRT-Hyst}$	PWM dimming		0.3		V
Burst Rate Generator						
Source Current	$I_{SRC(BRS)}$	V_{BRS} = 2V	120	150	180	µA
Lower Threshold	$V_{V(BRS)}$		2.2	2.4	2.6	V
Upper Threshold	$V_{P(BRS)}$		3.3	3.55	3.8	V

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_A = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply Current						
Supply Current (Enabled)	I_{IN-EN}	No driver output		1.5	2.5	mA
Supply Current (Disabled)	I_{IN-OFF}	V_{IN}=30V			1	µA
Operating Frequency	f_O	25kΩ LCS to GND	46	50	54	kHz
Frequency Set Voltage	V_{LCS}		1.1	1.2	1.3	V
Lamp Clock Control (LCC)						
LCC Enable Threshold	V_{LCC-EN}	Start Sweeping Frequency	0.8	0.9	1.0	V
LCC Source Current	I_{LCC-FT}	At Fault Condition, 25kΩ LCS to GND	44	48	51	µA
Frequency Increase Slope	$\Delta F_0/\Delta V_{LCC}$	0.9V<V_{LCC}<4.9V	14	15.5	17	kHz/V
Lamp Current Feedback (LI)						
Magnitude	$\|V_{LI}\|$		1.13	1.20	1.27	V
Sine Equivalent	V_{LI}			1.33		Vrms
Input resistance	R_{LI_IN}			60		kΩ
Lamp Voltage Feedbacks (LV)						
Open Lamp Voltage Feedback Threshold (Peak)	$V_{TH(LV)}$		2.2	2.4	2.6	V
Fault Timer						
Threshold	$V_{t(FT)}$		2.2	2.4	2.6	V
Sink Current	$I_{SINK(FT)}$			–1		µA
Open Lamp Source Current	$I_{PU\_OL(FT)}$			1		µA
Short Lamp Source Current	$I_{PU\_SL(FT)}$			100		µA
Comp						
Clamp Voltage	V_{COMP}			0.60		V
Reference Current	I_{COMP+}			20		µA
Reference Current at Fault Condition	$I_{COMP+FT}$	Fault Condition		3.7		µA
Pull Down Current at Voltage Regulation	$I_{COMP-VR}$	LV>2.4V		30		µA
Decay Current	I_{COMP-}	End of Burst		12		µA
Fault Detection Threshold (OLP, SLP, LI)						
OLP Threshold	V_{OLP}		2.2	2.4	2.6	V
SLP Threshold	V_{SLP}		2.2	2.4	2.6	V
SLP Detection Delay Time	T_{SLP}	Start when V_{COMP}>0.9V		400		us
LI threshold	V_{LI}		0.55	0.60	0.65	V
LI Detection Delay Time	T_{LI}	Start when V_{COMP}>0.9V		400		us
Output Gate Driver (VDRV)						
Voltage	V_{VDRV}	No load	8.7	9.7	10.4	V
Current	I_{VDRV}			20		mA

PIN FUNCTIONS

Pin #	Name	Description
1	OLP	Open Lamp Protection Input. A comparator is integrated in this pin for open lamp protection. If the voltage on this pin gets higher than 2.4V, the open lamp protection will be generated. It starts the fault timer by sourcing a 1uA current from FT pin, sweeps up the operating frequency by generating an internal current source flowing out of LCC pin, and disables the burst dimming.
2	LV	Lamp Voltage Feedback Input. The lamp voltage is sensed by this pin through a voltage divider from the hot end of the lamp to ground. If the voltage at LV exceeds +2.4 V, the COMP pin voltage is regulated to keep the lamp voltage at a high constant value. At the same time, the fault protection is triggered and the fault timer is started. The burst dimming is disabled when fault protection is triggered.
3	SLP	Short Lamp Protection Input. A comparator is integrated in this pin for short lamp protection. If the voltage on this pin gets lower than 2.4V for 400us (counting when V_{COMP}>0.9V), the short protection will be generated. It starts the fault timer by sourcing a 100uA current from FT pin, sweeps up the operating frequency by generating an internal current source flowing out of LCC pin, and disables the burst dimming. The reference for the lamp current feedback is lowered down to 1/6 in order to limit the short current. The protection function is disabled at burst off interval.
4	LI	Lamp Current Feedback Input. Connect this pin to the cold end of the lamp and shunt a sense resistor to ground. The internal error amplifier will sink a current from the COMP pin proportional to the absolute value of the voltage at this pin. The average of the absolute value of the voltage at this pin is regulated to 1.2V reference voltage. The voltage on this pin is also used for open lamp detection and protection. When the voltage on this pin gets lower than 0.6V for 400us (counting when V_{COMP}>0.9V), the IC recognize this as open lamp condition and generate a signal to sweep up the operating frequency and disable the burst dimming. At the same time, the fault protection is triggered and fault timer is started. At burst off interval, the detection and protection are disabled.
5	COMP	Feedback Compensation Node. Connect a compensation capacitor from this pin to GND.
6	FT	Fault Timer. Connect a timing capacitor from this pin to GND to set the fault timeout period. When the voltage on this pin gets higher than the 2.4V threshold, the IC latches up until EN is toggled.
7	LCC	Lamp Clock Control. The voltage on LCC will control the switching frequency. Connect a resistor paralleled with a capacitor from this pin to GND. If open lamp or short circuit is detected, an internal current will source from this pin. The sourcing current is determined by the LCS pin resistor. The voltage on this pin from 0.9V to 4.9V will linearly increase the operating frequency by 0 to 61kHz. LCC pin is also a flag that the fault condition is triggered.
8	LCS	Lamp Clock Set. Connect a resistor from this pin to GND. This resistor sets the operating frequency of the MP1006. A 25kOhm resistor sets the operating frequency at typical 50kHz.
9	BOSC	Burst Repetition Set. Connect a resistor in parallel with a capacitor from BOSC to GND. The resistor and capacitor programs the burst repetition rate and the minimum burst duty cycle. If the burst dimming is to be controlled by an external logic signal, pull up BOSC to VDRV through a 20kΩ resistor and apply the logic signal to the DBRT pin.
10	DBRT	Burst-Mode (Digital) Brightness Control Input. The voltage range from 0 V to 1.2V at DBRT linearly sets the burst-mode duty cycle from the minimum duty to 100%. For external PWM input dimming, directly apply the logic signal on this pin. The MP1006 has positive dimming polarity.
11	EN	Enable Input. Pull EN high to turn on the chip, and pull EN low to turn it off.

PIN FUNCTIONS *(continued)*

Pin #	Name	Description
12	VIN	Supply voltage input.
13	VDRV	Linear Regulator Output and Bias Supply of the Gate Driver. It provides the supply for the gate driver and also the external control circuit, the typical value is 9.7V. Bypass VDRV with a 1μF or larger ceramic capacitor.
14	GL	Driving signal output, 180 degree phase shifted of GR
15	GND	Ground.
16	GR	Driving signal output, 180 degree phase shifted of GL

OPERATION

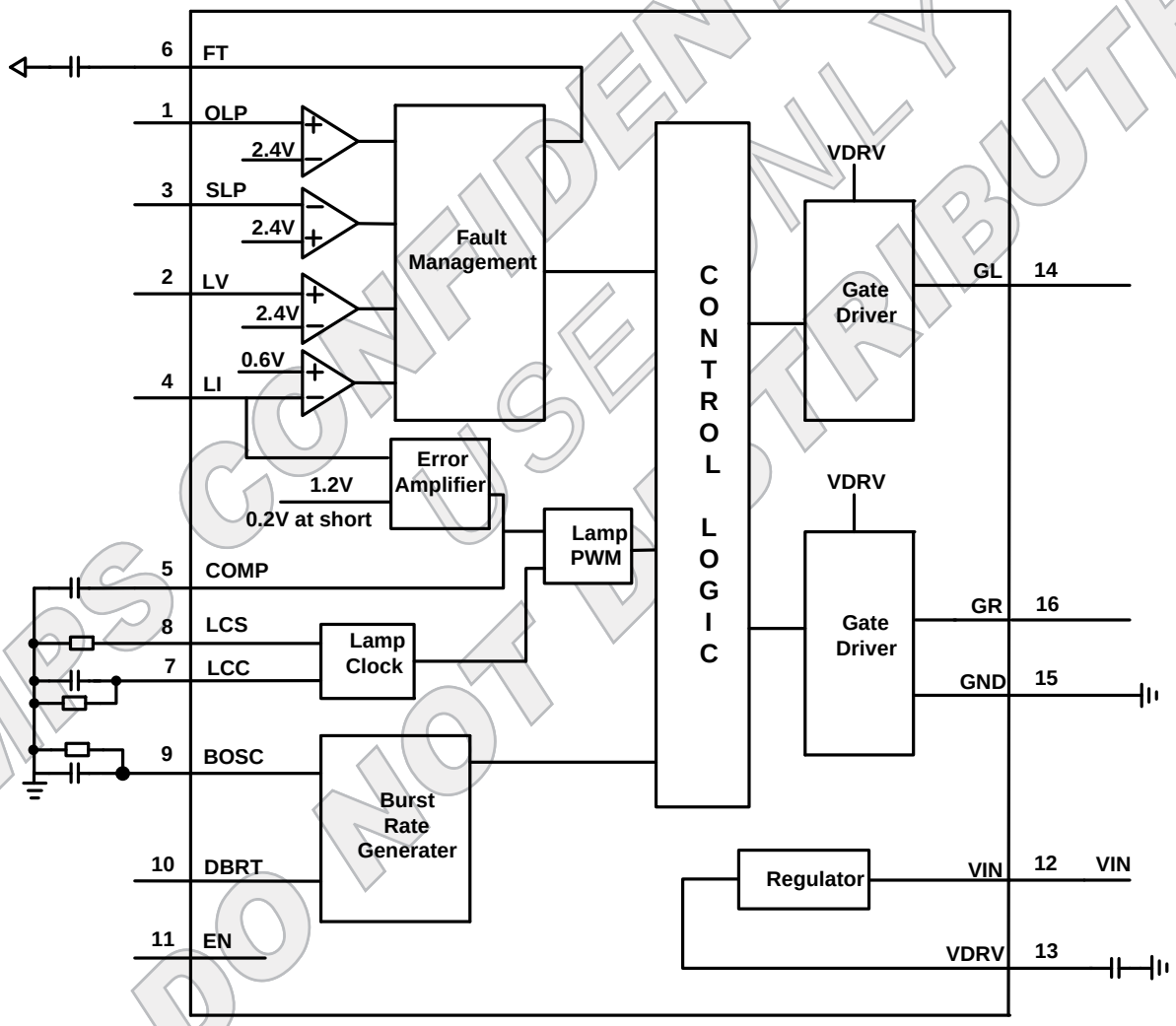


Figure 1—MP1006 Block Diagram

DESIGN INFORMATION

Steady State and Enable Control

The MP1006 is a fixed operating frequency off-line inverter controller specifically designed for the backlighting of multiple lamp liquid crystal displays (LCD). Powered by 9V to 30V input supplies, the MP1006 outputs two 180 degree phase shifted driving signals for the external power stages. Its enhanced 9V gate driver provides adequate driving capability to the external MOSFETs. It is able to directly drive the external gate driving transformer.

The operating frequency is set by an external resistor to minimize the possibility of interference with the refresh rate of the display. The operating frequency can be set by the resistor connected from LCS pin to GND.

The lamp striking frequency under open lamp condition is programmed by the LCC pin. The voltage on LCC in range of 0.9~4.9V linearly increases the operating frequency by 0 to 61kHz. When LCC voltage is lower than 0.9V, the operating frequency is not influenced.

The MP1006 utilizes PWM control to the inverter. The lamp current is sensed at LI pin and compared with internal reference. The internal error amplifier generates the error signal on COMP pin to control the PWM duty cycle. The full-wave lamp current sense amplifier provides superior output pulse symmetry and loop response time.

The system power is controlled by EN pin. When the chip is enabled, the built-in regulator for VDRV is powered up and the internal circuit starts.

Brightness Control

MP1006 implements burst dimming (digital brightness) of the lamp. Burst mode operation dims the lamp by modulating the duty cycle of a burst of AC lamp current and features soft-on/soft-off control of the lamp current envelope. The MP1006 has a built-in burst oscillator which can generate a triangle waveform on the BOSC pin. Burst dimming can be achieved by either a DC voltage input or external PWM signal. When burst dimming with a DC input voltage, add a capacitor in parallel with a resistor on BOSC pin to set the burst frequency and apply the DC voltage on the DBRT pin to program the burst duty cycle. When burst dimming with external PWM signal, pull up BOSC pin to VDRV through a 20kΩ resistor and apply the PWM signal on DBRT pin.

Fault Protection

System fault management facilities include the on-chip open-lamp detector and regulator, a dual mode fault timer and two smart comparators for open lamp and short circuit protection.

The lamp voltage is monitored by the LV pin through a capacitor divider, once the voltage on LV pin exceed 2.4V reference, the MP1006 will pull down the COMP voltage by a current pulse and reduce the power delivering to the power stage. Thus smoothly and stably regulate the lamp voltage to a user programmed striking voltage. At the same time when LV pin voltage hits the 2.4V threshold, the Open Lamp Mode is triggered.

At **Open Lamp Mode**, the IC generates an internal current source flowing out of the LCC pin. Together with the resistor connected from LCC to GND, a user programmed voltage is generated, which linearly increases the operating frequency. The LCC pin voltage in range of 0.9~4.9V linearly programs the frequency increase by 0 to 61kHz. The LCC pin internal current source is determined by the LCS pin resistor. And the capacitor on LCC pin helps to program the frequency sweeping speed. Meanwhile, a 1uA current source will charge the FT cap. If the voltage on FT pin exceeds 2.4V, the controller will shutdown and latch until the EN pin is toggled to restart the IC. Choose a proper capacitor on FT pin to obtain a desired timeout. In normal condition a 1μA sink current keeps the FT pin at 0V. During Open Lamp Mode, the IC ignores the burst control and runs continuously to ensure either the lamp has a chance to re-ignite or the fault timer can smoothly and accurately time out.

The lamp current feedback LI pin also functions as the open lamp detection. If the peak voltage on LI pin is lower than 0.6V for 400us (count when V_{COMP}>0.9V), the IC recognizes the lamp is open, and triggers the Open Lamp Mode. At burst dimming off interval, the fault detection on LI pin is disabled.

Two smart comparators are integrated for the open lamp and short circuit protection. It simplifies the protection design in multiple lamps application.

The OLP pin is used for open lamp protection. When the voltage on OLP pin is higher than 2.4V, the IC recognizes this as open lamp condition and triggers the Open Lamp Mode.

The SLP pin is used for short lamp protection. When the voltage on SLP pin is lower than 2.4V for 400us (count when V_{COMP}>0.9V), the IC recognizes it as short lamp condition and triggers the Short Lamp Mode. At burst dimming off interval, the fault detection on SLP pin is disabled.

At **Short Lamp Mode**, the IC also charges up the LCC pin to sweep up the frequency and ignores the burst dimming. It starts the short mode fault timer by sourcing a 100uA current to charge the FT capacitor, which is 100 times faster than that in the Open Lamp Mode. During Short Lamp Mode, the internal current feedback reference is reduced to 1/6 of the normal value, which helps for limiting the short circuit current to meet the safety requirement.

APPLICATION INFORMATION

Pin 1 (OLP):

Open Lamp Protection: This pin is used for open lamp protection, when the voltage on this pin is higher than 2.4V, the IC recognize this as open lamp condition and triggers Open Lamp Mode. Connect the signals which can indicate open lamp condition to this pin. The maximum lamp voltage, the maximum lamp voltage difference or the maximum lamp current difference are usually used to indicate the open lamp condition.

Pin 2 (LV):

Open Lamp Voltage Regulation: This pin is used for open lamp voltage regulation and open lamp protection. When the voltage on this pin exceeds 2.4V, an internal current source will discharge COMP to regulate the open lamp voltage. The regulated open lamp voltage is proportional to the ratio of the voltage divider in the voltage feedback. When LV voltage hits 2.4V, the IC recognizes this as open lamp condition and triggers Open Lamp Mode.

Pin 3 (SLP):

Short Lamp Protection: This pin is used for short lamp protection, when the voltage on this pin gets lower than 2.4V for 400us (Count when V_{COMP}>0.9V), the IC takes it as short lamp condition and triggers Short Lamp Mode. The minimum lamp voltage is usually used to indicate the short lamp condition.

Pin 4 (LI):

Lamp Current Regulation: This pin is used for Current regulation. The lamp current is fed back to the LI pin. The absolute voltage on this pin is regulated with 1.2V average value. For the sinusoid waveform on this pin, its RMS value is regulated to 1.33Vrms. At Short Lamp Mode, the reference voltage for LI is reduced to 0.2V (1/6) to limit the short circuit current.

LI pin also functions as open lamp detection, when the voltage on this pin gets lower than 0.6V for 400us (count when V_{COMP}>0.9V), the IC recognizes this as open lamp condition and triggers Open Lamp Mode.

Pin 5 (COMP):

This pin is used for compensation. Connect a 1~4.7nF capacitor from COMP to GND. This cap should be X7R ceramic. The value of this cap determines the stability of the lamp current regulation and open lamp voltage regulation. It also affects the soft-on rise time and soft-off fall time at burst dimming.

Pin 6 (FT):

Connect a capacitor from this pin to GND to set the fault timer.

Open Lamp Time Out:

$$C1 = \frac{t_{OPEN\ LAMP} \times 1\mu A}{2.4V}$$

For a C1 = 1uF, then the time out for open lamp will be 2.4 sec.

Short lamp Timeout: When Short Lamp Mode is triggered, the IC charges the FT cap with 100uA current. The short lamp timeout is about 1/100 of the open lamp timeout. To further reduce the short lamp timeout, modify the network at the FT pin as shown in Figure 2.

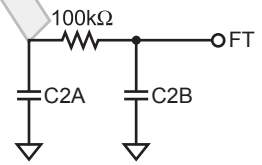


Figure 2—Timeout Adjustment

For C2B = 100nF, then the short lamp timeout is as short as 2.4ms.

Note: The open lamp time out will remain the same value as defined by C2A.

Pin 8 (LCS):

Connect a resistor from this pin to GND to set the lamp operating frequency (f_o). The value for this resistor R1 is calculated by

$$R1 = \frac{1.25 \times 10^9}{f_o}$$

For R1 = 25kΩ, operating clock will be 50kHz.

Pin 7 (LCC):

This pin is used to program the striking frequency at open lamp condition. The voltage on this pin in range of 0.9V~4.9V increases the operating frequency by 0~61 kHz, as shown in figure 3.

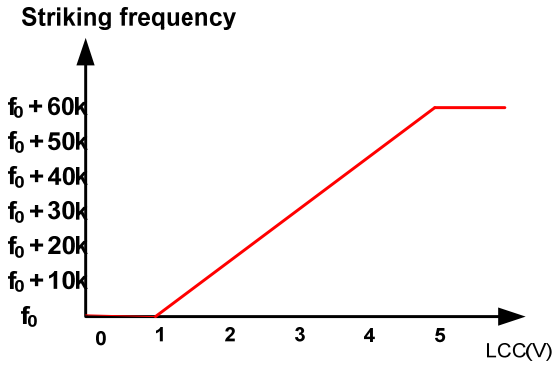


Figure 3—Striking Frequency vs. LCC Voltage

At Open Lamp Mode or Short Lamp Mode, an internal current source flows out of this pin. With a resistor in parallel with a capacitor on this pin, the IC softly sweeps up the striking frequency. The resistor determines the striking frequency value and the capacitor determines the sweeping speed. It helps to establish the striking voltage to ignite the lamp and also helps to eliminate the voltage spike by its soft sweeping.
The LCC voltage is:

$$V_{LCC} = \frac{1.2V}{R_{LCS}} \times R_{LCC}$$

The striking frequency is:

$$F_{strike} = F_{op} + (V_{LCC} - 0.9) \times 15.5 \times 10^3$$

The sweeping frequency can also be programmed externally by applying a voltage to LCC pin. At this condition, connect a 100Ω resistor on LCC pin to limit the flowing out current.

Pin 10 (DBRT):

This pin is used for burst brightness control. For DC input burst dimming, the DC voltage on this pin controls the burst percentage on the output. The signal is filtered for optimal operation. A voltage ranging from 0 to 1.2V on DBRT programs the burst dimming duty cycle from the minimum duty cycle to 100%.

For direct Pulse Width Modulation (PWM) burst dimming, Pull BOSC high to VDRV through a 20kΩ resistor and connect DBRT to a logic level PWM signal. Logic High is Burst On and a logic Low is Burst Off.

Pin 9 (BOSC):

BOSC pin is used to set the burst dimming frequency. Connect a resistor (R2) in parallel with a capacitor (C3) on this pin to set the burst dimming frequency and the minimum burst on time: t_{MIN}, as shown in figure 4.

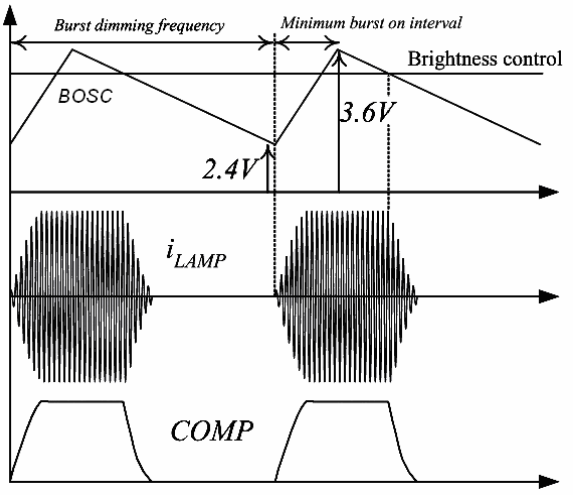


Figure 4—Burst Mode with DC Input Voltage at DBRT Pin

Set t_{MIN} to achieve the minimum required system brightness. Ensure that t_{MIN} is long enough that the lamp does not extinguish.

These values are determined as follows:

Select a Minimum Duty Cycle, D_{MIN}, where:

$$D_{MIN} = t_{MIN} \times f_{Burst}$$

R2 and C3 are determined by:

$$R2 \approx 21.16k\left(\frac{1}{D_{MIN}} - 1\right) + 21.43k$$

$$C3 = \frac{1 - D_{MIN}}{f_{Burst} \times R2 \times 0.405}$$

For D_{MIN} = 0.1, f_{Burst} = 200Hz, then R2 = 212k, C3 = 52nF

For direct PWM burst dimming, pull BOSC high to VDRV through a 20kΩ resistor and apply the PWM signal to DBRT pin.

Table 1—Function Mode

Function	Pin Connection	
	DBRT	BOSC
Burst Mode with DC Input Voltage	0V to 1.2V	C3, R2
Burst Mode with External Source	PWM	To VDRV through 20kΩ resistor

Burst Brightness Polarity: 100% duty cycle at DBRT voltage 1.2V.

Pin 11 (EN):

Pull this pin high to enable the chip, and pull it low to disable the chip.

Pin 12 (VIN):

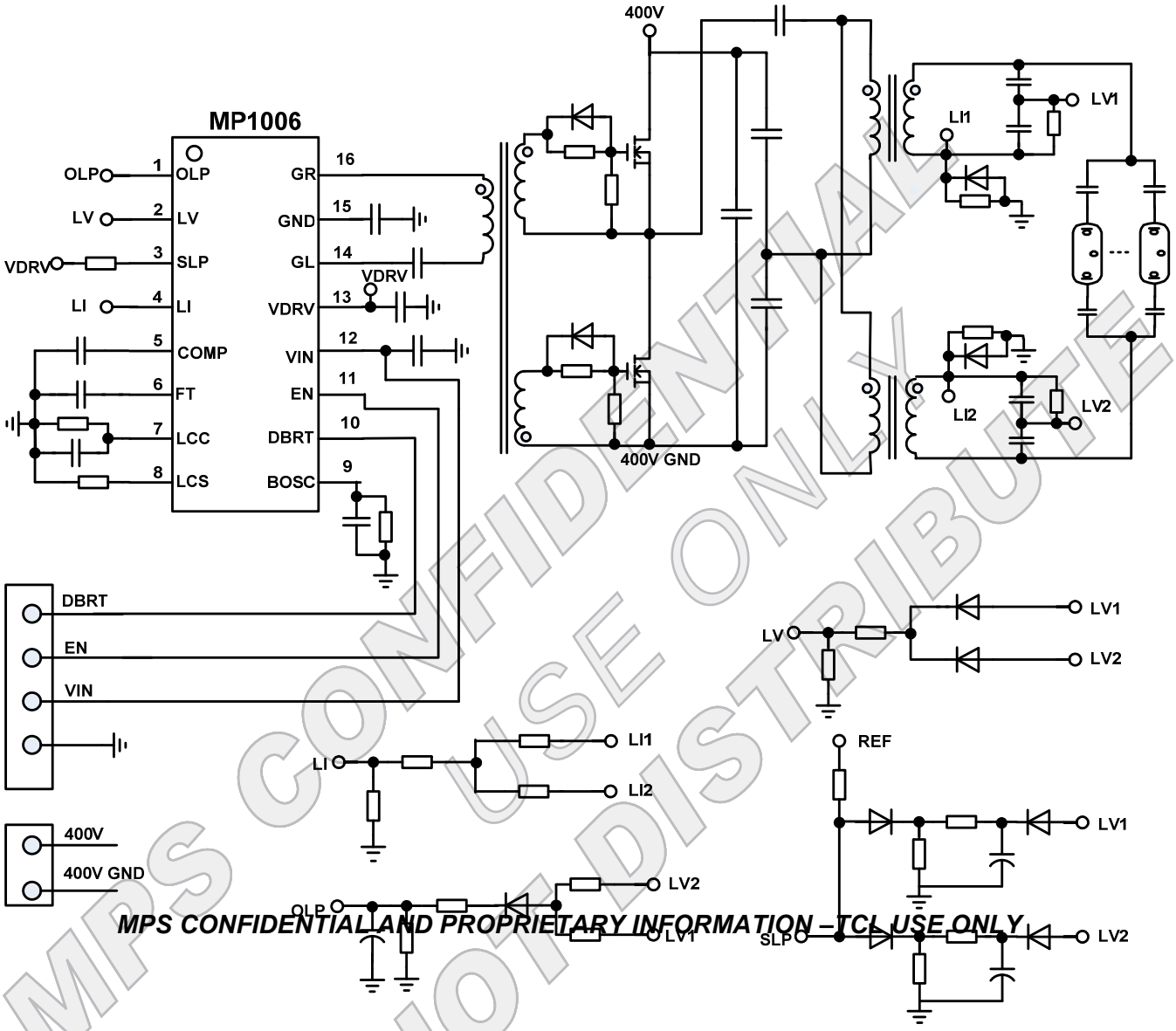
Supply voltage input. By pass the supply voltage with a 0.1uF or greater ceramic cap. This cap should be placed close to the IC.

Pin 13 (VDRV):

This pin provides the gate driver supply voltage, its typical value is 9.7V. Connect a 1uF or greater ceramic capacitor on this pin to bypass the supply voltage. This voltage is also used to supply the external control circuit.

Pin 14(GL), Pin 16 (GR):

Gate driving signals output. GL and GR are 180 degree phase shifted driving signals. With its enhanced driving capability, GL and GR are able to directly drive the externally MOSFET in the off-line system through a gate driving transformer. Connect two 5Ω resistors in series with GL and GR to eliminate the EMI noise injected to the IC.



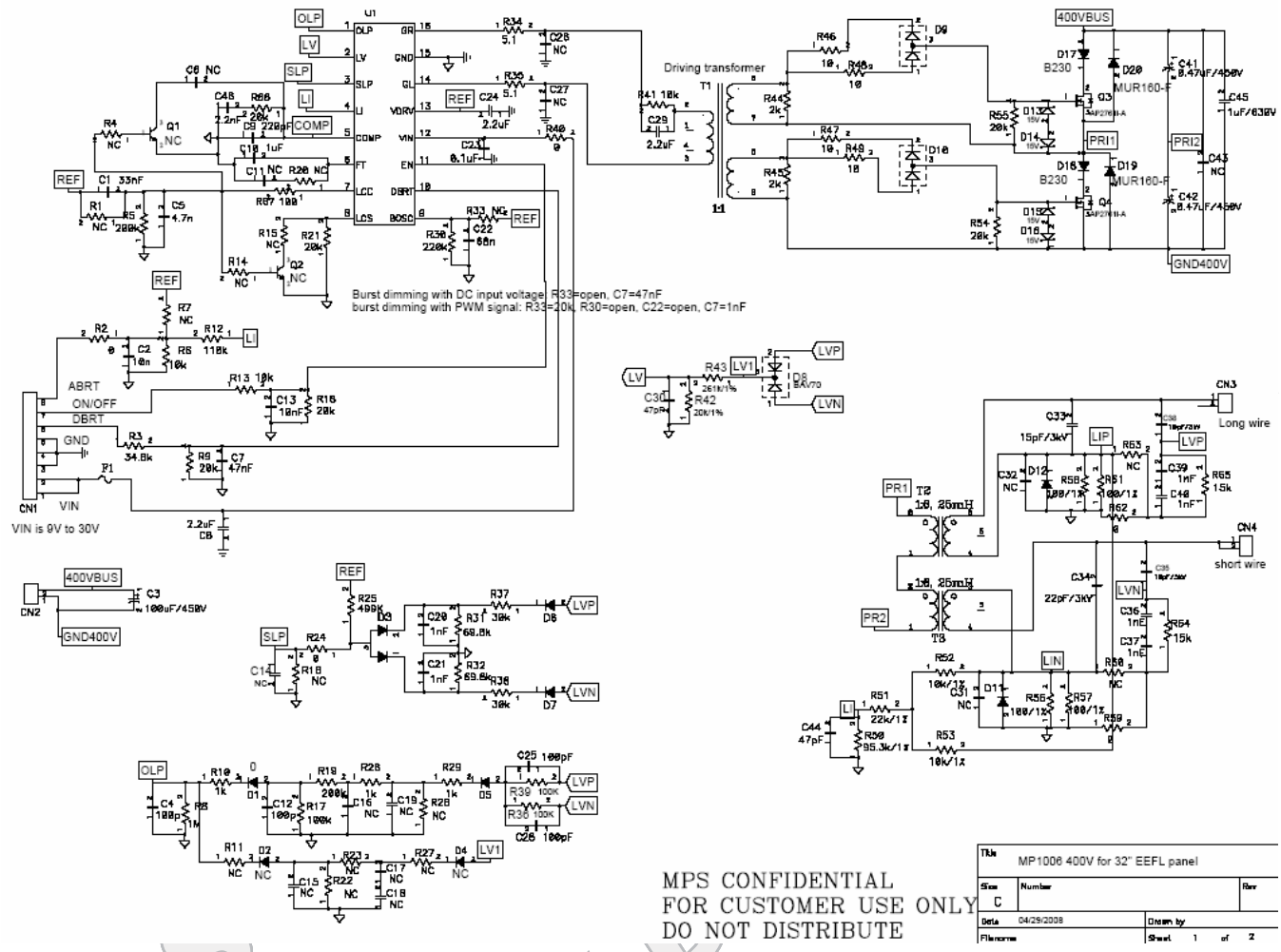
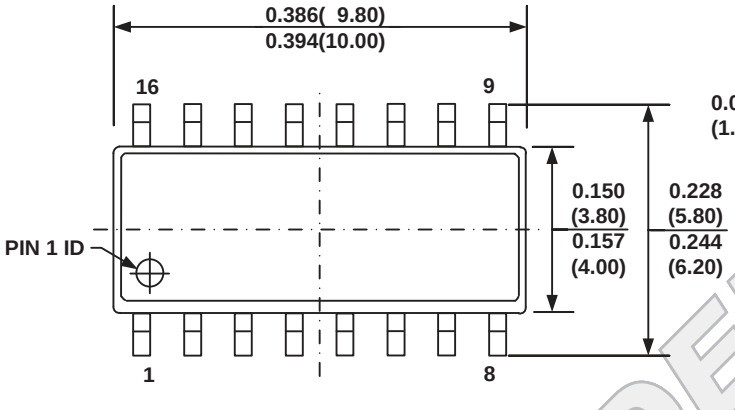


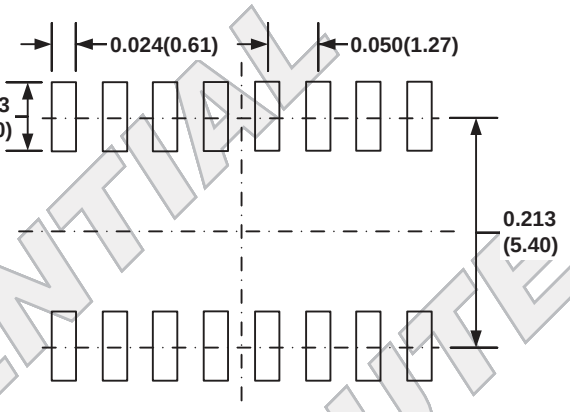
Figure 6—MP1006 400V EEFL Driver for 32” Panel

PACKAGE INFORMATION

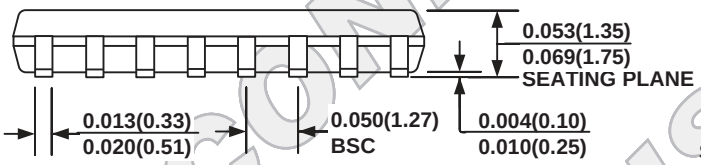
SOIC16



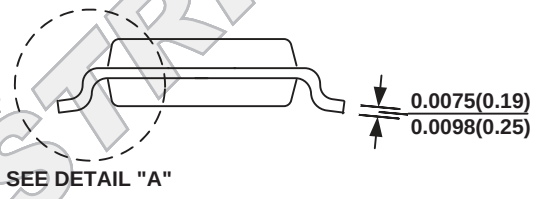
TOP VIEW



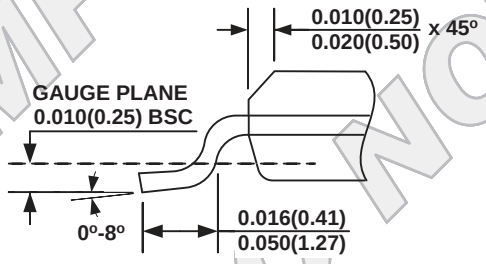
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AC.
6) DRAWING IS NOT TO SCALE.