iNTEGRATED MEMORY LOGIC

iML7991

Programmable Gamma Buffers, DVR & VCOM buffer with Embedded Non Volatile Memory (NVM)

General Description

The iML7991 is an I^2C interfaced digitally programmable gamma buffer and digital VR (DVR) with integrated VCOM buffer & contains embedded programmable Non Volatile Memory (NVM). NVM can be used to hold the digital values corresponding to 14 programmable GAMMA channel and DVR

14 channels of programmable and switchable reference voltage generator provide switching between 2 GAMMA curves. With these gamma curves, DVR & internal VCOM with embedded Non Volatile Memory (NVM), the iML7991 provides a complete 14-channel total gamma solution for TFT-LCD displays.

Through the I^2C interface, user can program the DVR_OUT, which connects to the input of the V_{COM} Buffer, to fine tune the V_{COM} setting. Also the serial interface allows user to optimize the 14-channel switchable gamma reference voltages to enhance the display performance.

An external resistor attached to the SET pin sets the full-scale sink current and determines the lowest voltage of the V_{COM} input. At power up, the iML7991 automatically sets the 7-bit DVR register value and 10bit 14 channel gamma buffer values to the values stored in NVM. Gamma buffer outputs are not enabled until all values are read from NVM.

The iML7991 is available in a 32-pin 5x5 Thin QFN package with a maximum thickness of 0.8mm for ultra thin LCD panel design.

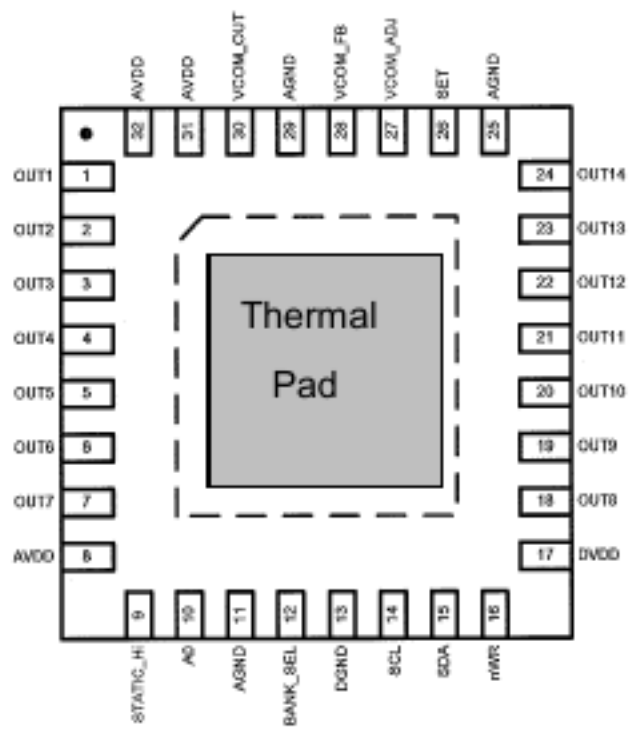
Applications

- TFT-LCD TVs
- TFT-LCD Monitors
- TFT-LCD Notebook PC

Ordering Information

Package	Part Number	Tape & Reel
32-pin TQFN (Halogen Free)	iML7991ID	-
	iML7991ID-TR	13”

Pin Diagrams (Top View)



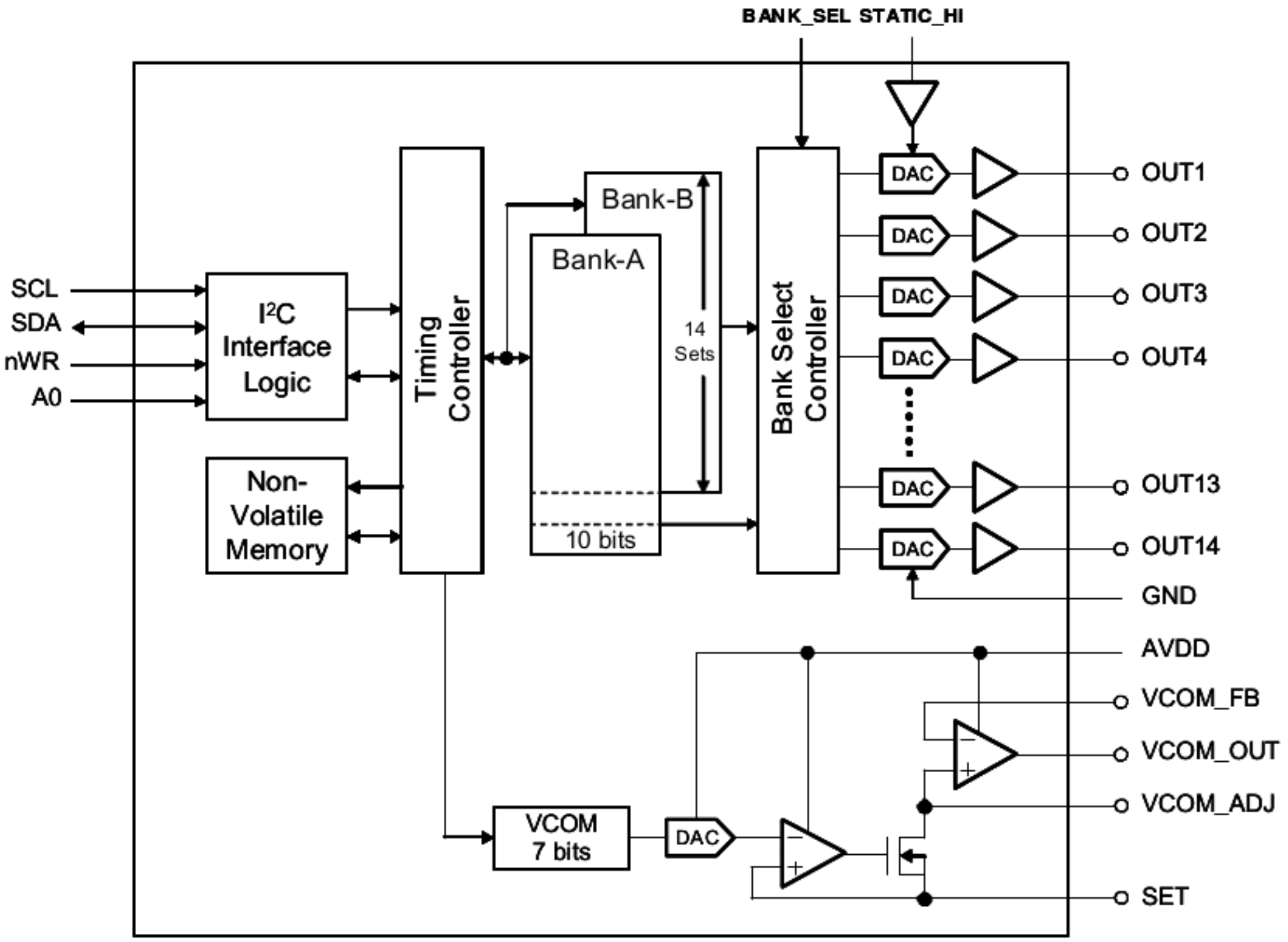
Features

- 128-step programmable sink-current output for DVR_OUT
- DVR_OUT voltage adjustable via SET Pin
- Built in VCOM buffer
- Guaranteed monotonic over temperature for DVR_OUT and Gamma Buffer outputs
- 14-ch analog output for gamma reference voltages with 10 bit DAC resolution
- 1024 -step digitally programmable gamma reference voltages
- 1 STATIC_HI voltage input used as upper reference voltage for internal DAC operation.
- Digital Supply Voltage(DVDD): 2.3V to 4V
  - NVM Read: Minimim DVDD 2.3V
  - NVM write : Minimum DVDD 2.7V
- Analog Supply Voltage (AVDD): 6.5V to 18V
- I^2C Interface:
  - Address: 111010A_0C (A_0 → bit-0 address = 0 or 1)
    (C=0 → Write; C=1 → Read.)
  - 400KHz maximum clock frequency
- 32-TQFN (0.85mm max) with thermal pad

Pin Descriptions

Pin No.	Pin Name	Type	I/O Type	Function
8,31,32	AVDD	Power	Supply	Analog power supply
11,25,29	AGND	Ground	Ground	Analog Ground
15	SDA	Digital	Input and Open Drain Output	I^2C Serial Digital Data Input/Output.
14	SCL	Digital	Input	I^2C Digital Serial Clock Input
27	VCOM_ADJ	Analog	Output	Adjust sink current output. This pin connects to resistive divider between AVDD and AGND that sets VCOM voltage
30	VCOM_OUT	Analog	Output	Voltage output for VCOM.
28	VCOM_FB	Analog	Input	VCOM feedback signal
26	SET	Analog	Input	Full scale sink current adjustment
16	nWR	Digital	Input	Enable/Disable write data in Non Volatile Memory. nWR = 0, Data can be written to Non Volatile Memory nWR = 1, Data can not be written to Non Volatile Memory
1	OUT1	Analog	Output	Analog output reference-1
2	OUT2	Analog	Output	Analog output reference-2
3	OUT3	Analog	Output	Analog output reference-3
4	OUT4	Analog	Output	Analog output reference-4
5	OUT5	Analog	Output	Analog output reference-5
6	OUT6	Analog	Output	Analog output reference-6
7	OUT7	Analog	Output	Analog output reference-7
18	OUT8	Analog	Output	Analog output reference-8
19	OUT9	Analog	Output	Analog output reference-9
20	OUT10	Analog	Output	Analog output reference-10
21	OUT11	Analog	Output	Analog output reference-11
22	OUT12	Analog	Output	Analog output reference-12
23	OUT13	Analog	Output	Analog output reference-13
24	OUT14	Analog	Output	Analog output reference-14
17	DVDD	Power	Supply	Digital voltage power supply
13	DGND	Ground	Ground	Digital Ground
12	BANK_SEL	Digital	Input	Internal A/B bank select, LO=Bank A, HI=Bank B
9	STATIC_HI	Analog	Input	Hi reference for output voltage
10	A0	Digital	Input	Device address select (A0 low address 0x74, A0 High address 0x75)
	TP	Thermal Pad	-	Thermal pad connected to AGND

Function Block Diagram



Absolute Maximum Ratings

Caution: Values beyond absolute ratings can cause the device to be prematurely damaged.
Absolute maximum ratings are stress ratings only and functional device operation is not guaranteed.

DVDD to GND	-0.3 to + 7V	**Operating Temperature**	-40°C to +85°C
Input Voltages to GND: **VCOM_FB,VCOM_ADJ,SET** **BANK_SEL,A0,SCL,SDA,nWR**	 - 0.3V to +20V -0.3V to +7V	**ESD (HBM) Rating: Device**	±2KV
Output Voltage to GND: OUT	- 0.3V to + 20V	**Moisture Sensitivity**	Level-1
Maximum Continuous Output Current **Out1 to out14** **VCOM**	 -60 to +60mA -130 to +130mA	**Max. Lead Temperature (soldering 10sec) (Lead Tips Only)**	+260°C
Max. Storage Temperature Range	-65°C to +150°C	**Max. Junction Temperature Range**	+150°C

***Note**: All parameters having Min/Max specifications are guaranteed. Typical values are for reference purpose only. Unless otherwise noted, all tests are pulsed tests at the specified temperature, therefore: $T_J = T_C = T_A$.*

Electrical Characteristics

Test Conditions: DVDD = 3V, AVDD = 16.5V, @T_A = 25°C unless otherwise specified.

Parameter	Symbol	Test Conditions	Temp (°C)	Min	Typ	Max	Units
DC CHARACTERISTICS							
DVDD Supply Range (Operating)	D_{VDD}		Full	2.3	-	3.6	V
DVDD Supply voltage for NVM read operation		NVM Read		2.3	3.3	3.6	V
DVDD Supply voltage for NVM write operation		NVM write		2.7	3.3	3.6	V
DVDD Supply Current	I_{DD}	DVR &Gamma Registers are at default values (No load)	Full	-	1	-	mA
AVDD Supply Range	V_{AVDD}	DVDD range 2.3V – 3.6V	Full	6.5	-	18	V
AVDD Supply Current	I_{AVDD}	DVR &Gamma Registers are at default values (No load)	Full	-	25	-	mA
Gamma Voltage Resolution	GM_{VR}		Full	-	10	-	Bits
Gamma Differential Nonlinearity	GM_{DN}	Monotonic over temperature	Full	- 1		+1	LSB
Gamma Integral Nonlinearity	GM_{IN}		Full	- 4		+4	LSB
SET Voltage Resolution	SET_{VR}		Full	-	7	-	Bits
SET Differential Nonlinearity	SET_{DN}	Monotonic over temperature	Full	-1	-	+1	LSB
SET Zero-Scale Error	SET_{ZSE}		Full	-1	-	+2	LSB
SET Full-Scale Error	SET_{FSE}		Full	-4	-	+4	LSB
SET Current	I_{SET}	Through R_{SET}	Full	-	-	120	µA
AVDD to SET voltage attenuation	$V_{AVDDSET}$		Full	0.05	-	-	V/V
SDA, SCL Input Logic High	V_{IH}		Full	0.7 * DVDD	-	-	V
SDA, SCL Input Logic Low	V_{IL}		Full	-	-	0.3 * DVDD	V

Parameter	Symbol	Test Conditions	Temp (°C)	Min	Typ	Max	Units
SDA, SCL Hysteresis	HYS_{swp}		Full	0.05 * DVDD			V
SDA Output Logic High	VOHS	@ I_L = + 3 mA	Full	DVDD - 0.4			V
SDA Output Logic Low	VOLS	@ I_L = -3 mA	Full			0.4	V
I^2C INTERFACE							
SCL Clock Frequency	F_{SCL}		Full	0	-	400	kHz
I^2C Clock High Time	t_{SCH}		Full	0.6			µs
I^2C Clock Low Time	t_{SCL}		Full	1.3			µs
I^2C spike rejection filter pulse width	t_{DSP}		Full	0		50	ns
I^2C Data Set-up Time	t_{SDS}		Full	100			ns
I^2C Data Hold Time	t_{SDH}		Full	0		900	ns
I^2C SDA, SCL Input Rise Time	t_{I2CR}	Load dependent	Full	20 + 0.1* CB		1000	ns
I^2C SDA, SCL Input Fall Time	t_{I2CF}	Load dependent	Full	20 + 0.1* CB		300	ns
I^2C bus free time between stop and start	t_{BUF}		Full	1.3			µs
I^2C repeated start condition set-up	t_{STS}		Full	0.6			µs
I^2C repeated start condition hold	t_{STH}		Full	0.6			µs
I^2C Stop Condition Set-up	t_{SPS}		Full	0.6			µs
I^2C Bus Capacitive Load	CB		Full			400	pF
Capacitance on SDA	C_{SDA}		Full			10	pF
GAMMA BUFFER & VCOM BUFFER							
Output High (OUT1 to OUT7)	V_{OH}	No load DAC = 1023	Full		STATIC_HI		V
Output Low (OUT1 to OUT7)	V_{OL}	No load DAC = 0	Full	1.5			V
Output High (OUT8 to OUT14)	V_{OH}	No load DAC = 1023	Full		STATIC_HI -1.5		V
Output Low (OUT8 to OUT14)	V_{OL}	No load DAC = 0	Full	0			mV
Output current	Iout	GAMMA Buffer	Full		±25		mA
		VCOM Buffer	Full		±100		mA
Output Short circuit current	Isc	GAMMA Buffer	Full		±75		mA
		VCOM Buffer	Full		±140		mA
Slew Rate	SR	GAMMA Buffer@10K,10pf	Full		8		V/µs
		VCOM Buffer	Full		20		V/µs
Load Regulation	REG	I_{OUT}=5mA step @default values	Full		0.4		mV/mA
Power Supply Rejection Ratio	PSRR	AVDD sweeps from 14V to 16V	Full	50	60		dB

I²C Operation:

Write Mode

If the read/write bit =low @ I2C protocol, the device enter the write mode, and the Host can write data into register part, including CONTROL BYTE, VCOM register, DAC_Reg. if the RESET, WR to NVM bit of Control Byte is "1", iML7991 internal H/W will return "NA" if the host try to write registers.

Burst Mode Write Operation

For the burst mode in the write transfer, a master device sends data to program all the output buffers. The input data bytes (DATA 1 (MSB) and (DATA 1 (LSB)) to the first channel (OUT1) starts from the third byte following the control byte and DVR byte. The second channel (OUT2) is programmed by the fifth and sixth byte (DATA 2 (MSB) and (DATA 2 (LSB)), and so on. Each byte is followed by an acknowledge bit.

Single Mode Write operation

The device also support single mode transfer, a master device send data to program define output buffer. The input data bytes (DATA N (MSB) and (DATA N (LSB)) to the N channel (OUT N). Each byte is followed by an acknowledge bit.

Write protocols

If internal memory operation is already in progress then device will return No Acknowledgment, i.e. NA to any of I2C host command to indicate that memory operation is in process.

In following protocols:
S indicates START
P Indicates STOP
A indicates ACKNOWLEDGEMENT
NA indicates NO ACKNOWLEDGEMENT
SR indicates REPEAT START
R indicates READ
W indicate WRITE

Write protocol to load EEPROM data to registers:

S	Slave Address	W	A	Index Address 0	A	Control Byte | (0x10)	A	P

Write protocol to write registers data to EEPROM:

S	Slave Address	W	A	Index Address 0	A	Control Byte | (0x08)	A	P

Write protocol to enable outputs:

S	Slave Address	W	A	Index Address 0	A	Control Byte | (0x02)	A	P

Write protocol to write data to DVCOM:

S	Slave Address	W	A	Index Address 1	A	Control Byte | (0x02)	A	P

Single Mode Write Protocol to write register at index address X:

Consist of 3 steps:

Step 1: Disable output by resetting OUT_EN bit

S	Slave Address	W	A	Index Address 0	A	Control Byte (0x00)	A	P

Step 2: Write data for registers X, X ≥ 2

S	Slave Address	W	A	Index Address X	A	MSB(X)	A	LSB(X)	A	P

Step 3: Enable output by setting OUT_EN bit

S	Slave Address	W	A	Index Address 0	A	Control Byte (0x02)	A	P

Note: Step 1 and 3 are not mandatory for step 2 and depends on application to use them or not.

Burst Mode Write Protocol to write from register at index address X to index address Y:

Consist of 3 steps:

Step 1: Disable output by resetting OUT_EN bit

S	Slave Address	W	A	Index Address 0	A	Control Byte (0x00)	A	P

Step 2: Write data for registers X

S	Slave Address	W	A	Index Address X	A	MSB(X)	A	LSB(X)	A	---

--	A	MSB(Y)	A	LSB(Y)	A	P

Step 3: Enable output by setting OUT_EN bit

S	Slave Address	W	A	Index Address 0	A	Control Byte (0x02)	A	P

Note: Step 1 and 3 are not mandatory for step 2 and depends on application to use them or not.

Read protocols

If internal memory operation is already in progress then device will return No Acknowledgment, i.e. NA to any of I2C host command to indicate that memory operation is in process.

In following protocols

S indicates START

P Indicates STOP

A indicates ACKNOWLEDGEMENT

NA indicates NO ACKNOWLEDGEMENT

SR indicates REPEAT START

R indicates READ

W indicate WRITE

Read protocol to read control byte (index address 0) or DVCOM (index address 1)

S	Slave Address	W	A	Index Address 0/1	SR	Slave Address	R	A	DATA 0/1	NA	P

Single Mode Read Protocol to read register at index address X:

Read data for registers X, X ≥ 2

S	Slave Address	W	A	Index Address X	SR	Slave Address	R	A	Data for X	NA	P

Burst Mode Read Protocol to Read from register at index address X to index address Y:

S	Slave Address	W	A	Index Address X	SR	Slave Address	R	A	DATA(X)	A	DATA(X+1)	A	----

----------	A	DATA (Y-1)	A	Data(Y)	NA	P

Index Address Table

iML7991 Device Address 0x74, 0x75										
Index Address	DATA								BANK	Note
Hex	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0		
00	CTRL BYTE[7:0]									CTRL BYTE
01	DVR[7:0]									DIGITAL VCOM
02	-	-	G1[9]	G1[8]	G1[7]	G1[6]	G1[5]	G1[4]	BANK A	GAMMA 1/2
03	G1[3]	G1[2]	G1[1]	G1[0]	-	-	G2[9]	G2[8]	BANK A	
04	G2[7]	G2[6]	G2[5]	G2[4]	G2[3]	G2[2]	G2[1]	G2[0]	BANK A	
05	-	-	G3[9]	G3[8]	G3[7]	G3[6]	G3[5]	G3[4]	BANK A	GAMMA 3/4
06	G3[3]	G3[2]	G3[1]	G3[0]	-	-	G4[9]	G4[8]	BANK A	
07	G4[7]	G4[6]	G4[5]	G4[4]	G4[3]	G4[2]	G4[1]	G4[0]	BANK A	
08	-	-	G5[9]	G5[8]	G5[7]	G5[6]	G5[5]	G5[4]	BANK A	GAMMA 5/6
09	G5[3]	G5[2]	G5[1]	G5[0]	-	-	G6[9]	G6[8]	BANK A	
0A	G6[7]	G6[6]	G6[5]	G6[4]	G6[3]	G6[2]	G6[1]	G6[0]	BANK A	
0B	-	-	G7[9]	G7[8]	G7[7]	G7[6]	G7[5]	G7[4]	BANK A	GAMMA 7/8
0C	G7[3]	G7[2]	G7[1]	G7[0]	-	-	G8[9]	G8[8]	BANK A	
0D	G8[7]	G8[6]	G8[5]	G8[4]	G8[3]	G8[2]	G8[1]	G8[0]	BANK A	
0E	-	-	G9[9]	G9[8]	G9[7]	G9[6]	G9[5]	G9[4]	BANK A	GAMMA 9/10
0F	G9[3]	G9[2]	G9[1]	G9[0]	-	-	G10[9]	G10[8]	BANK A	
10	G10[7]	G10[6]	G10[5]	G10[4]	G10[3]	G10[2]	G10[1]	G10[0]	BANK A	
11	-	-	G11[9]	G11[8]	G11[7]	G11[6]	G11[5]	G11[4]	BANK A	GAMMA 11/12
12	G11[3]	G11[2]	G11[1]	G11[0]	-	-	G12[9]	G12[8]	BANK A	
13	G12[7]	G12[6]	G12[5]	G12[4]	G12[3]	G12[2]	G12[1]	G12[0]	BANK A	
14	-	-	G13[9]	G13[8]	G13[7]	G13[6]	G13[5]	G13[4]	BANK A	GAMMA 13/14
15	G13[3]	G13[2]	G13[1]	G13[0]	-	-	G14[9]	G14[8]	BANK A	
16	G14[7]	G14[6]	G14[5]	G14[4]	G14[3]	G14[2]	G14[1]	G14[0]	BANK A	
17 TO 24	R	R	R	R	R	R	R	R	BANK A	RESERVED
25	-	-	G1[9]	G1[8]	G1[7]	G1[6]	G1[5]	G1[4]	BANK B	GAMMA 1/2
26	G1[3]	G1[2]	G1[1]	G1[0]	-	-	G2[9]	G2[8]	BANK B	
27	G2[7]	G2[6]	G2[5]	G2[4]	G2[3]	G2[2]	G2[1]	G2[0]	BANK B	
28	-	-	G3[9]	G3[8]	G3[7]	G3[6]	G3[5]	G3[4]	BANK B	GAMMA 3/4
29	G3[3]	G3[2]	G3[1]	G3[0]	-	-	G4[9]	G4[8]	BANK B	
2A	G4[7]	G4[6]	G4[5]	G4[4]	G4[3]	G4[2]	G4[1]	G4[0]	BANK B	

Index Address	DATA								BANK	Note
2B	-	-	G5[9]	G5[8]	G5[7]	G5[6]	G5[5]	G5[4]	BANK B	
2C	G5[3]	G5[2]	G5[1]	G5[0]	-	-	G6[9]	G6[8]	BANK B	GAMMA 5/6
2D	G6[7]	G6[6]	G6[5]	G6[4]	G6[3]	G6[2]	G6[1]	G6[0]	BANK B	
2E	-	-	G7[9]	G7[8]	G7[7]	G7[6]	G7[5]	G7[4]	BANK B	
2F	G7[3]	G7[2]	G7[1]	G7[0]	-	-	G8[9]	G8[8]	BANK B	GAMMA 7/8
30	G8[7]	G8[6]	G8[5]	G8[4]	G8[3]	G8[2]	G8[1]	G8[0]	BANK B	
31	-	-	G9[9]	G9[8]	G9[7]	G9[6]	G9[5]	G9[4]	BANK B	
32	G9[3]	G9[2]	G9[1]	G9[0]	-	-	G10[9]	G10[8]	BANK B	GAMMA 9/10
33	G10[7]	G10[6]	G10[5]	G10[4]	G10[3]	G10[2]	G10[1]	G10[0]	BANK B	
34	-	-	G11[9]	G11[8]	G11[7]	G11[6]	G11[5]	G11[4]	BANK B	
35	G11[3]	G11[2]	G11[1]	G11[0]	-	-	G12[9]	G12[8]	BANK B	GAMMA 11/12
36	G12[7]	G12[6]	G12[5]	G12[4]	G12[3]	G12[2]	G12[1]	G12[0]	BANK B	
37	-	-	G13[9]	G13[8]	G13[7]	G13[6]	G13[5]	G13[4]	BANK B	
38	G13[3]	G13[2]	G13[1]	G13[0]	-	-	G14[9]	G14[8]	BANK B	GAMMA 13/14
39	G14[7]	G14[6]	G14[5]	G14[4]	G14[3]	G14[2]	G14[1]	G14[0]	BANK B	
3A TO 45	R	R	R	R	R	R	R	R	BANK B	RESERVED

NOTE: Above GX[N] means Gamma buffer number X bit number N

Control Register Definition: 8 bit Control register exist at index address 0

Bits	Bit Name	Description
0	---	This bit is reserved
1	OUT_EN	This bit when SET to 1 enables outputs
2	---	This bit is reserved
3	WR_NVM	This bit when SET to 1, bank A & bank B data is written to EEPROM
4	RESET	This bit when SET to 1, bank A & bank B data is read from EEPROM
5	----	This bit is reserved
6	HOT_EN	This bit when SET to 1 disables thermal sensor
7	----	This bit is reserved

NOTE:

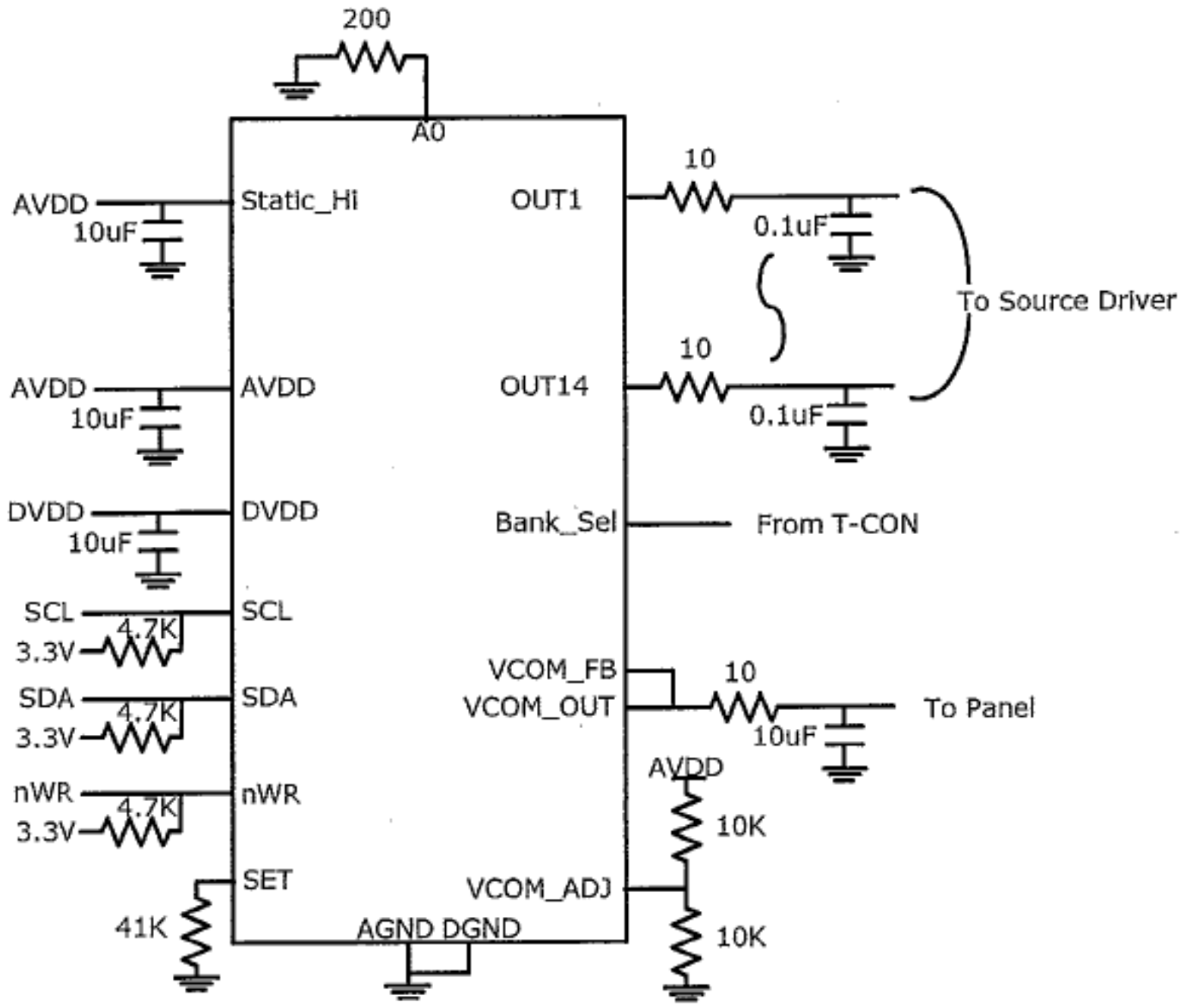
WR_NVM & RESET bit when set to 1 memory operation starts. After memory operation is finished these bits are cleared by hardware to 0.

RESET bit when set to 1, OUT_EN bit is cleared by hardware to disable outputs. When memory read is finished, OUT_EN is set to 1 by hardware to enable the outputs again.

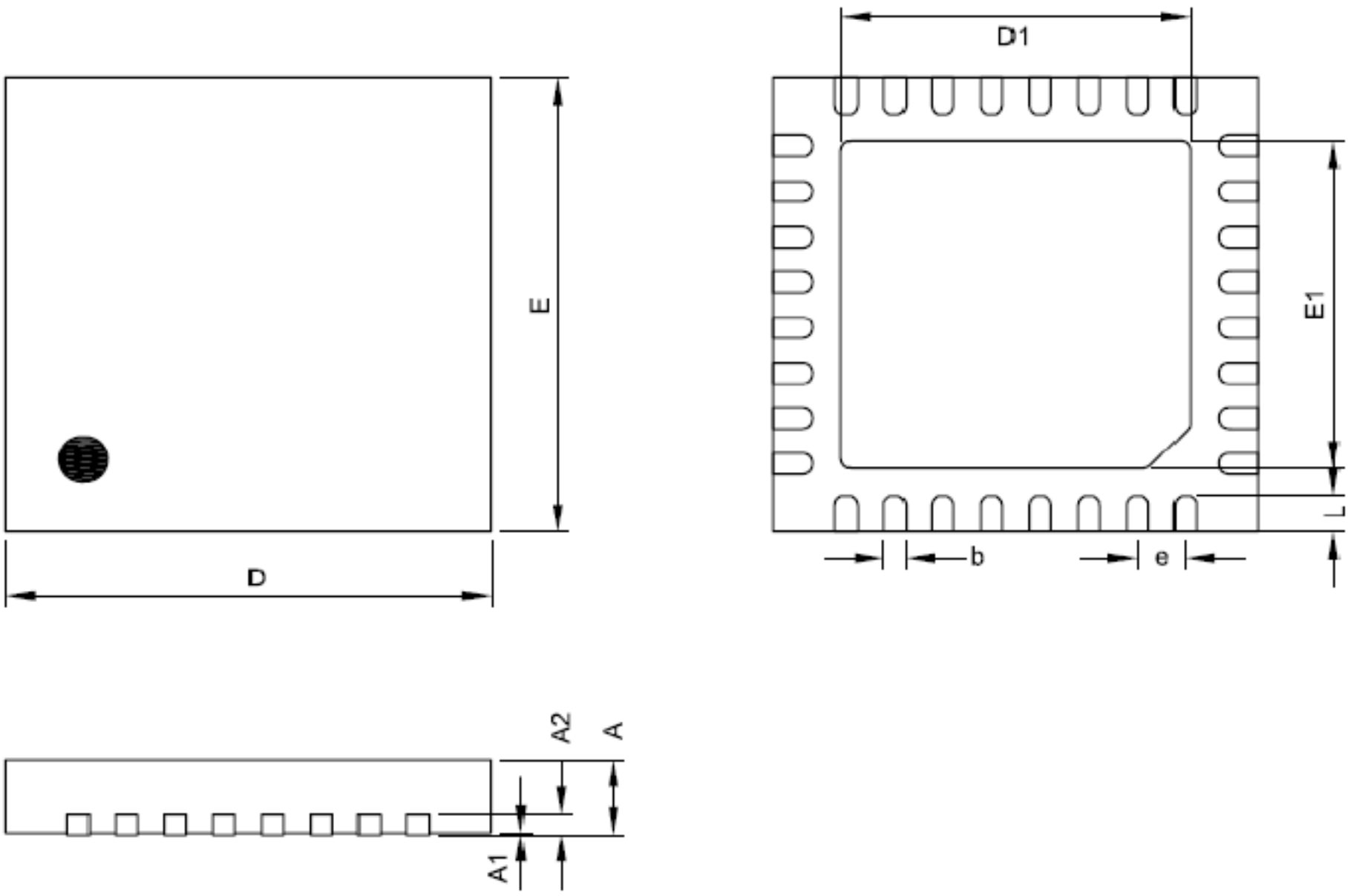
Power-On Sequencing

At power-on, before DVDD stabilizes, make sure that AVDD always trails DVDD (i.e. DVDD voltage level should be higher than AVDD during power-on) to avoid AVDD in-rush current. It is strongly recommended to power on DVDD first before turning on AVDD.

Typical Application Circuit



Package Information 32 Pin TQFN



Symble	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.0276	0.0295	0.0315
A1	0.00	---	0.05	0.0000	---	0.0020
A2	0.19	0.20	0.21	0.0075	0.0079	0.0083
D	4,95	5,00	5,05	0,1949	0,1969	0,1988
E	4,95	5,00	5,05	0,1949	0,1969	0,1988
D1	3.50	3.65	3.75	0.1378	0.1437	0.1476
E1	3.50	3.65	3.75	0.1378	0.1437	0.1476
b	0.18	0.23	0.28	0.0071	0.0091	0.0110
e	0,50 BSC			0,0197 BSC		
L	0,30	0,35	0,45	0,0118	0,0138	0,0177