ESS Technology, Inc.

PRELIMINARY

ES6008/18/28/38
Vibratto™ DVD Processor Solutions
Data Sheet

DESCRIPTION

Built on ESS's proprietary and flexible Programmable Multimedia Processor architecture, the Vibratto™ series of DVD processors combine audio/video stream data processing, system control and housekeeping functions, video postprocessing, and display format encoding, enabling various DVD-based multimedia electronics to be built with minimal external components. The Vibratto series includes new features for DVD-Audio support, progressive scan video output, and built-in TV encoder and video DACs.

All of the Vibratto DVD processors each include two parallel processing units, a RISC processor, a vector engine, and supplemental hardware resources for implementing specialized encoding and decoding tasks in the device architectures. All of these resources are interconnected with two separate data buses, each with its own DMA unit and interface to external memory. The processing units enable simultaneous parallel execution of system commands and data processing.

Both the RISC processor and vector engine are independently programmable. Each has its own on-chip cache memory. The RISC processor and its associated hardware units perform bit stream parsing, control audio data output, transfer video and audio data to the vector engine and service system control and housekeeping functions. The vector engine and associated hardware units perform audio and video microcode processing required by A/V standards such as Dolby Digital™, DTS™, MPEG and JPEG. These processing tasks include audio DSP, video motion compensation and estimation, loop filtering, discrete cosine transforms (DCT) and inverse DCT, quantization and inverse quantization.

The Vibratto DVD processors support both JPEG/MP3 audio playback and the Kodak PictureCD JPEG display format. These new features allow Picture CDs created with images and voiceovers from digital cameras to be enjoyed in a DVD player or Home Theater System.

All of the Vibratto DVD processors support both parallel and serial DVD loader interfaces for system MPEG A/V data stream input, industry standard-I^2S bus for audio data input and output, direct system EPROM and SDRAM access for high-speed command fetching and audio/video data buffering and processing. The Vibratto DVD processors are available in 208-pin Plastic Quad Flat Pack (PQFP) device packages.

FEATURES

- Dedicated core and I/O power supplies for low-power operation; integrated 32-bit RISC processor for system host, eliminating requirements of an external host CPU
- Supports DVD-Video, DVD-Audio, VideoCD 1.1, 2.0, and 3.0, Super VideoCD (SVCD), CD-DA, MP3, and Kodak Picture-CD
- Supports parallel and serial interfaces to ATAPI, Compact Flash, DCI, IDE and UDF DVD loaders
- Direct interface of 8- or 16-bit SDRAM of up to 128-Mb capacity at a variety of speed grades
- Direct interface of up to 4 banks of 8- or 16-bit EPROM or Flash EPROM; automatic firmware updating of Flash EPROM through DVD loader

Video

- Built-in NTSC/PAL encoder includes field-adaptive de-interlacing for progressive scan video output for clearer and more stable display *(ES6028 and ES6038 Only)*
- Macrovision 7.1 and Macrovision AGC 1.03 compliant video outputs for 480-pixel progressive scan and for NTSC/PAL interlaced video
- Four built-in 10-bit Video DACs provide simultaneous video outputs of composite and S-video, or composite and YUV; supports selectable 8-bit CCIR 601 4:2:2 YUV outputs
- 8-bit On-Screen Display (OSD) controller with 3-bit blending provides display with 256 colors in 8 degrees of transparency
- On-chip Subpicture Unit (SPU) decoder supports karaoke lyric, subtitles, and EIA-608 compliant Line 21 Captioning
- Video error concealment, motion zoom and pan and NTSC to PAL and PAL to NTSC conversion supported

Audio

- Dolby Digital (AC-3), DVD-Audio, Pro Logic, DTS, MPEG-1 layer 2 and 3 Audio (MP3), and High-Definition Compatible Digital™ (HDCD) decoding
- On-chip Dolby Digital (AC-3) and DTS 5.1 channel decoding and output *(ES6018/28/38 Only)*
- Dolby Digital and DTS S/PDIF digital audio output.
- Dolby Digital Class A, DTS, and HDCD certified
- Meridian Lossless Packing™ (MLP) decoding and Linear PCM for DVD-Audio *(ES6038 Only)*

CONTENTS

FIGURES

TABLES

SYSTEM BLOCK DIAGRAM

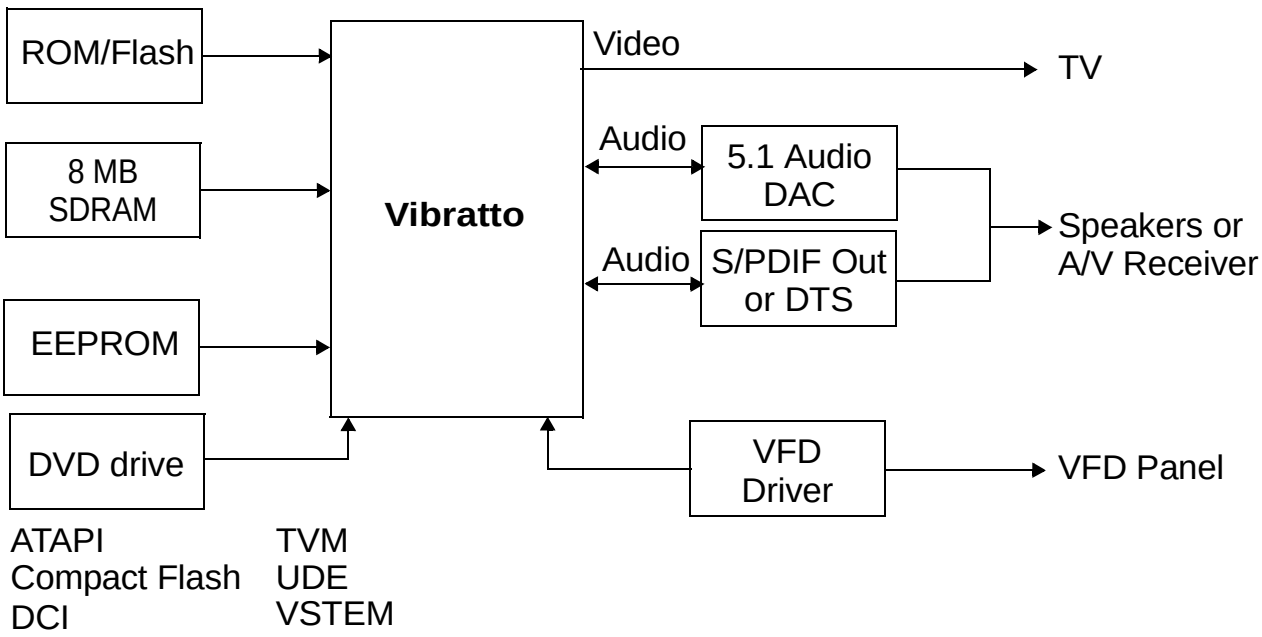


Figure 1 Vibratto System Block Diagram

ES60X8 PINOUT DIAGRAM

The identical device pinouts for the ES6008, ES6018, ES6028 and ES6038 are shown in Figure 2.

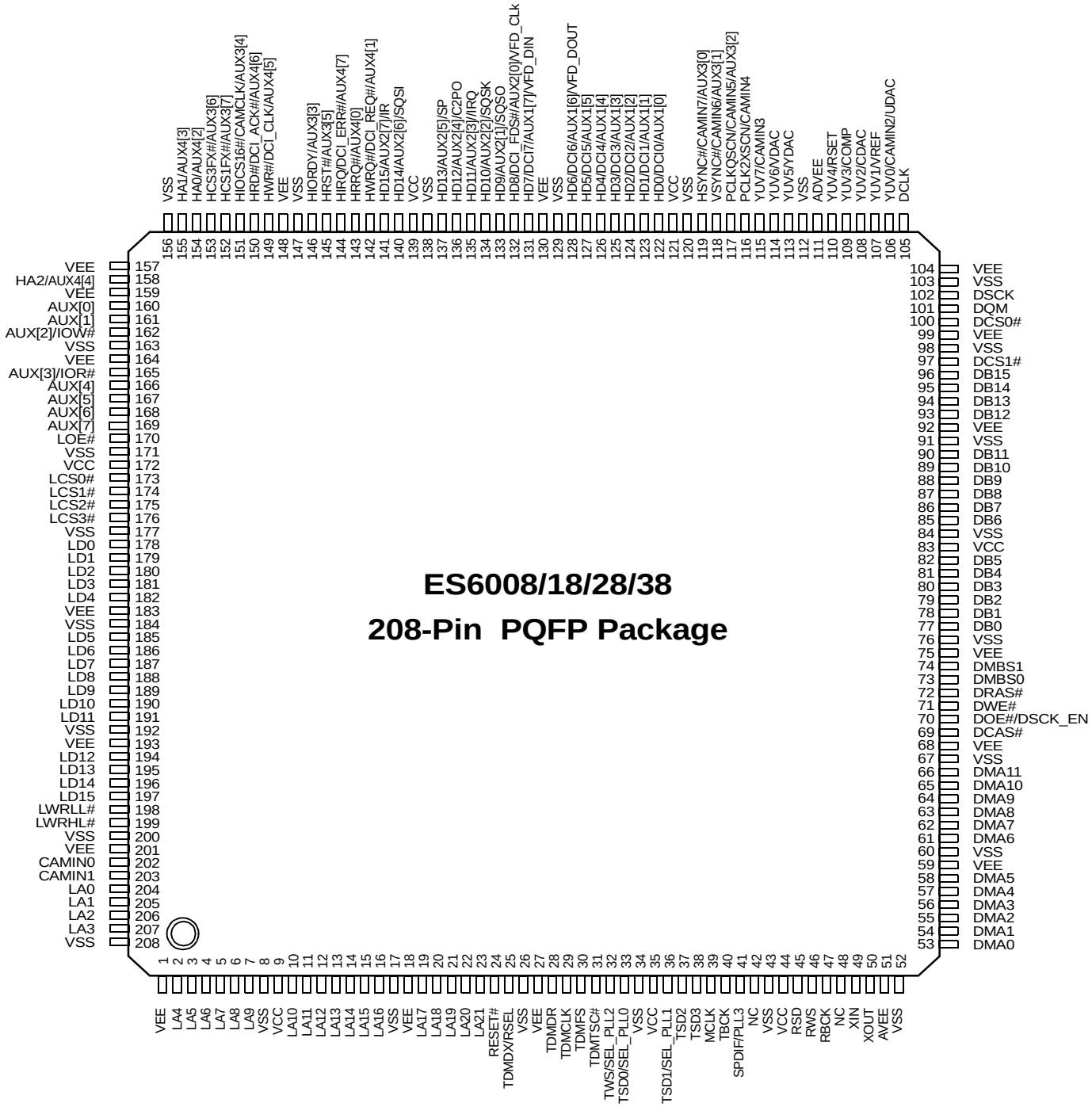


Figure 2 ES60x8 Pinout

ES60X8 PIN DESCRIPTION

Table 1 lists the identical pin descriptions for the ES6008, ES6018, ES6028 and ES6038.

Table 1 ES60x8 Pin Description

<table>
<tr><th>Name</th><th>Number</th><th>I/O</th><th>Definition</th></tr>
<tr><td>VEE</td><td>1,18, 27, 59, 68, 75, 92, 99, 104, 130, 148, 157, 159, 164, 183, 193, 201</td><td>I</td><td>I/O power supply.</td></tr>
<tr><td>VSS</td><td>8, 17, 26, 34, 43, 52, 60, 67, 76, 84, 91, 98, 103, 112, 120, 129, 138, 147, 156, 163, 171, 177, 184, 192, 200, 208</td><td>I</td><td>Ground.</td></tr>
<tr><td>LA[21:0]</td><td>23:19, 16:10, 7:2, 207:204</td><td>O</td><td>Device address output.</td></tr>
<tr><td>VCC</td><td>9, 35, 44, 83, 121, 139, 172</td><td>I</td><td>Core power supply.</td></tr>
<tr><td>RESET#</td><td>24</td><td>I</td><td>Reset input, active low.</td></tr>
<tr><td>TDMDX</td><td rowspan="2">25</td><td>O</td><td>TDM transmit data.</td></tr>
<tr><td>RSEL</td><td>I</td><td>ROM Select.
<table>
<tr><th>RSEL</th><th>Selection</th></tr>
<tr><td>0</td><td>16-bit ROM</td></tr>
<tr><td>1</td><td>8-bit ROM</td></tr>
</table></td></tr>
<tr><td>TDMDR</td><td>28</td><td>I</td><td>TDM receive data.</td></tr>
<tr><td>TDMCLK</td><td>29</td><td>I</td><td>TDM clock input.</td></tr>
<tr><td>TDMFS</td><td>30</td><td>I</td><td>TDM frame sync.</td></tr>
<tr><td>TDMTSC#</td><td>31</td><td>O</td><td>TDM output enable.</td></tr>
<tr><td>TWS</td><td rowspan="2">32</td><td>O</td><td>Audio transmit frame sync.</td></tr>
<tr><td>SEL_PLL2</td><td>I</td><td>System and DSCK output clock frequency selection is made at the rising edge of RESET#. The matrix below lists the available clock frequencies and their respective PLL bit settings.
<table>
<tr><th>SEL_PLL2</th><th>SEL_PLL1</th><th>SEL_PLL0</th><th>Clock Type</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>VCO off.</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>DCLK</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Bypass mode</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>DCLK x 2</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>DCLK x 4.5</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>DCLK x 3</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>DCLK x 3.5z</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>DCLK x 4</td></tr>
</table></td></tr>
<tr><td>TSD0</td><td rowspan="2">33</td><td>O</td><td>Audio transmit serial data port 0.</td></tr>
<tr><td>SEL_PLL0</td><td>I</td><td>Refer to the description and matrix for SEL_PLL2 pin 32.</td></tr>
<tr><td>TSD1</td><td rowspan="2">36</td><td>O</td><td>Audio transmit serial data port 1.</td></tr>
<tr><td>SEL_PLL1</td><td>I</td><td>Refer to the description and matrix for SEL_PLL2 pin 32.</td></tr>
<tr><td>TSD[2]</td><td>37</td><td>O</td><td>Audio transmit serial data output 2.</td></tr>
<tr><td>TSD[3]</td><td>38</td><td>O</td><td>Audio transmit serial data output 3.</td></tr>
</table>

Table 1 ES60x8 Pin Description (Continued)

<table>
<tr><th>Name</th><th>Number</th><th>I/O</th><th>Definition</th></tr>
<tr><td>MCLK</td><td>39</td><td>I/O</td><td>Audio master clock for audio DAC.</td></tr>
<tr><td>TBCK</td><td>40</td><td>O</td><td>Audio transmit bit clock.</td></tr>
<tr><td>SPDIF</td><td rowspan="2">41</td><td>O</td><td>S/PDIF output.</td></tr>
<tr><td>SEL_PLL3</td><td>I</td><td>Clock source select.
<table><tr><th>SEL_PLL3</th><th>Clock Source</th></tr><tr><td>0</td><td>Crystal oscillator</td></tr><tr><td>1</td><td>DCLK input</td></tr></table></td></tr>
<tr><td>NC</td><td>42, 48</td><td></td><td>No connect pins. Leave open.</td></tr>
<tr><td>RSD</td><td>45</td><td>I</td><td>Audio receive serial data.</td></tr>
<tr><td>RWS</td><td>46</td><td>I</td><td>Audio receive frame sync.</td></tr>
<tr><td>RBCK</td><td>47</td><td>I</td><td>Audio receive bit clock.</td></tr>
<tr><td>XIN</td><td>49</td><td>I</td><td>Crystal input.</td></tr>
<tr><td>XOUT</td><td>50</td><td>O</td><td>Crystal output.</td></tr>
<tr><td>AVEE</td><td>51</td><td>I</td><td>Analog power for PLL.</td></tr>
<tr><td>DMA[11:0]</td><td>66:61, 58:53</td><td>O</td><td>DRAM address bus [11:0].</td></tr>
<tr><td>DCAS#</td><td>69</td><td>O</td><td>DRAM column address strobe.</td></tr>
<tr><td>DOE#</td><td rowspan="2">70</td><td>O</td><td>DRAM output enable.</td></tr>
<tr><td>DSCK_EN</td><td>O</td><td>DRAM clock enable.</td></tr>
<tr><td>DWE#</td><td>71</td><td>O</td><td>DRAM write enable.</td></tr>
<tr><td>DRAS#</td><td>72</td><td>O</td><td>DRAM row address strobe.</td></tr>
<tr><td>DMBS0</td><td>73</td><td>O</td><td>SDRAM bank select 0.</td></tr>
<tr><td>DMBS1</td><td>74</td><td>O</td><td>SDRAM bank select 1.</td></tr>
<tr><td>DB[15:0]</td><td>96:93, 90:85, 82:77</td><td>I/O</td><td>DRAM data bus [15:0].</td></tr>
<tr><td>DCS[1:0]#</td><td>97,100</td><td>O</td><td>SDRAM chip select [1:0].</td></tr>
<tr><td>DQM</td><td>101</td><td>O</td><td>Data input/output mask.</td></tr>
<tr><td>DSCK</td><td>102</td><td>O</td><td>Output clock to SDRAM.</td></tr>
<tr><td>DCLK</td><td>105</td><td>I</td><td>27 MHz clock input to PLL.</td></tr>
<tr><td>YUV0</td><td rowspan="3">106</td><td>O</td><td>YUV0 pixel output data.</td></tr>
<tr><td>CAMIN2</td><td>I</td><td>Camera input 2.</td></tr>
<tr><td>UDAC</td><td>O</td><td>Video DAC output.
<table><tr><th>Mode</th><th>YDAC</th><th>UDAC</th><th>VDAC</th><th>CDAC</th></tr><tr><td>A</td><td>Y</td><td>C</td><td>Composite</td><td>C</td></tr><tr><td>B</td><td>Y</td><td>Composite</td><td>Composite</td><td>C</td></tr><tr><td>C</td><td>Y</td><td>U</td><td>Composite</td><td>V</td></tr><tr><td>D</td><td>Y</td><td>U</td><td>C</td><td>V</td></tr></table>Y: Luma component for YUV and Y/C processing.
C: Chrominance signal for Y/C processing.
U: Chrominance component signal for YUV mode.
V: Chrominance component signal for YUV mode.</td></tr>
</table>

Table 1 ES60x8 Pin Description (Continued)

Name	Number	I/O	Definition
YUV1	107	O	YUV1 pixel output data.
VREF		I	Internal voltage reference to video DAC. Bypass to ground with 0.1 µF capacitor.
YUV2	108	O	YUV2 pixel output data.
CDAC		O	Video DAC output. Refer to description and matrix for UDAC pin 106.
YUV3	109	O	YUV3 pixel output data.
COMP		I	Compensation input. Bypass to ADVEE with 0.1 µF capacitor.
YUV4	110	O	YUV4 pixel output data.
RSET		I	DAC current adjustment resistor input.
ADVEE	111	I	Analog power for video DAC.
YUV5	113	O	YUV5 pixel output data.
YDAC		O	Video DAC output. Refer to description and matrix for UDAC pin 106.
YUV6	114	O	YUV6 pixel output data.
VDAC		O	Video DAC output. Refer to description and matrix for UDAC pin 106.
YUV7	115	O	YUV7 pixel output data.
CAMIN3		I	Camera YUV 3.
PCLK2XSCN	116	I/O	27-MHz video output pixel clock.
CAMIN4		I	Camera YUV 4.
PCLKQSCN	117	O	13.5-MHz video output pixel clock.
CAMIN5		I	Camera YUV 5.
VSYNC#	118	I/O	Vertical sync, active low.
CAMIN6		I	Camera YUV 6.
HSYNC#	119	I/O	Horizontal sync, active low.
CAMIN7		I	Camera YUV 7.
HD[5:0]	127:122	I/O	Host data I/O [5:0].
DCI[5:0]		I/O	DVD channel data I/O [5:0].
AUX1[5:0]		I/O	Aux1 data I/O [5:0].
HD[6]	128	I/O	Host data I/O [6].
DCI[6]		I/O	DVD channel data I/O [6].
AUX1[6]		I/O	Aux1 data I/O [6].
VFD_DOUT		I	VFD data output.
HD[7]	131	I/O	Host data I/O [7].
DCI[7]		I/O	DVD channel data I/O [7].
AUX1[7]		I/O	Aux1 data I/O [7:0].
VFD_DIN		I	VFD data input.
HD[8]	132	I/O	Host data bus 8.
DCI_FDS#		I/O	DVD input sector start.
AUX2[0]		I/O	Aux2 data I/O 0.
VFD_CLK		I	VFD clock input.
HD[9]	133	I/O	Host data bus line 9.
AUX2[1]		I/O	Aux2 data I/O [1] when selected.
SQSQ		I	Subcode-Q data.
HD[10]	134	I/O	Host data bus line10.
AUX2[2]		I/O	Aux2 data I/O [2] when selected.
SQSK		I	Subcode-Q clock.

Table 1 ES60x8 Pin Description (Continued)

Name	Number	I/O	Definition
HD[11]	135	I/O	Host data bus line11.
AUX2[3]		I/O	Aux2 data I/O [3] when selected.
IRQ		O	IRQ output.
HD[12]	136	I/O	Host data bus line12.
AUX2[4]		I/O	Aux2 data I/O [4] when selected.
C2PO		I	C2PO error correction flag from CD-ROM.
HD[13]	137	I/O	Host data bus line13.
AUX2[5]		I/O	Aux2 data I/O [5] when selected.
SP		I	16550 UART serial port input.
HD[14]	140	I/O	Host data bus line14.
AUX2[6]		I/O	Aux2 data I/O [6] when selected.
SQSI		I	Subcode-Q sync.
HD[15]	141	I/O	Host data bus line15.
AUX2[7]		I/O	Aux2 data I/O [7] when selected.
IR		I	IR remote control input.
HWRQ#	142	O	Host write request.
DCI_REQ#		O	DVD control interface request.
AUX4[1]		I/O	Aux4 data I/O 1.
HRRQ#	143	O	Host read request.
AUX4[0]		I/O	Aux4 data I/O 0.
HIRQ	144	I/O	Host interrupt.
DCI_ERR#		I/O	DVD channel data error.
AUX4[7]		I/O	Aux4 data I/O 7.
HRST#	145	O	Host reset.
AUX3[5]		I/O	Aux3 data I/O 5.
HIORDY	146	I	Host I/O ready.
AUX3[3]		I/O	Aux3 data I/O 3.
HWR#	149	I/O	Host write.
DCI_CLK		I/O	DVD channel data clock.
AUX4[5]		I/O	Aux4 data I/O 5.
HRD#	150	O	Host read.
DCI_ACK#		O	DVD channel data valid.
AUX4[6]		I/O	Aux4 data I/O 6.
HIOCS16#	151	I	Device 16-bit data transfer.
CAMCLK		I	Camera port pixel clock input.
AUX3[4]		I/O	Aux3 data I/O 4.
HCS1FX#	152	O	Host select 1.
AUX3[7]		I/O	Aux3 data I/O 7.
HCS3FX#	153	O	Host select 3.
AUX3[6]		I/O	Aux3 data I/O 6.
HA[2:0]	158, 155:154	I/O	Host address bus.
AUX4[4:2]		I/O	Aux4 data I/Os [4:2].
AUX[1:0]	160	I/O	Auxiliary ports 1:0.

Table 1 ES60x8 Pin Description (Continued)

Name	Number	I/O	Definition
AUX[2]	162	I/O	Auxiliary port 2.
IOW#		O	I/O Write strobe.
AUX[3]	165	I/O	Auxiliary port 3.
IOR#		O	I/O Read strobe.
AUX[7:3]	169:166	I/O	Auxiliary ports 7:3.
LOE#	170	O	Device output enable.
LCS[3:0]#	176:173	O	Chip select [3:0].
LD[15:0]	197:194, 191:185, 182:178	I/O	EPROM device data bus.
LWRLL#	198	O	Device low-byte write enable.
LWRHL#	199	O	Device high-byte write enable.
CAMIN0	202	I	Camera YUV 0.
CAMIN1	203	I	Camera YUV 1.

LICENSING REQUIREMENTS

Dolby Digital Licensing

Dolby Digital audio enabling software is provided with the Vibratto series of DVD processors. Dolby is a trademark of the Dolby Laboratories. Supply of this implementation of Dolby Technology does not convey a license or imply a right under any patent, or any other Industrial or Intellectual Property Right of Dolby Laboratories, to use this implementation in any end-user or ready-to-use final product. Companies planning to use this implementation in products must obtain a license from Dolby Laboratories Licensing Corporation before designing such products. Additional per-chip royalties may be required and are to be paid by the purchaser to Dolby Laboratories, Inc. Details of the OEM Dolby Digital license may be obtained by writing to:

Dolby Laboratories Inc.
Dolby Laboratories Licensing Corporation
Attn.: Intellectual Property Manager
100 Potrero Avenue
San Francisco, CA 94103-4813

Macrovision Licensing

Macrovision Copy Protection is supported in the Vibratto series of DVD processors. The use of Macrovision's Copy Protection technology in the device must be authorized by Macrovision and is intended for home and other limited pay-per-view uses only, unless otherwise authorized in writing by Macrovision.

Reverse engineering or disassembly is prohibited. A valid Macrovision license must be in effect between the Vibratto purchaser and Macrovision Corporation. Additional per-chip royalties may be required and are to be paid by the purchaser to Macrovision Corporation. Details of the Macrovision license may be obtained by writing to:

Macrovision Corporation
1341 Orleans Avenue
Sunnyvale, CA 94089

FUNCTIONAL DESCRIPTION

Figure 3 shows the internal block diagram for the basic Vibratto DVD processor.

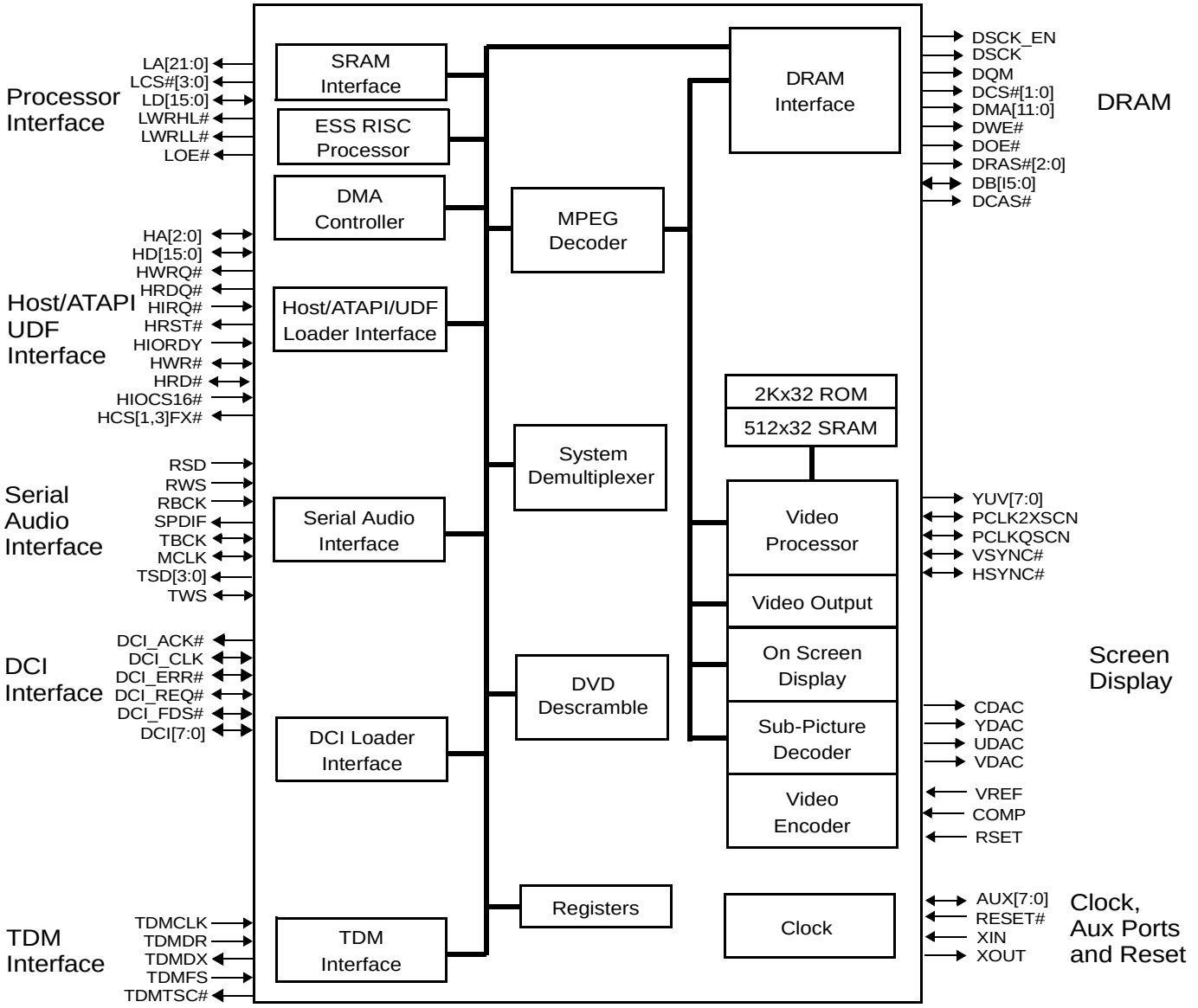


Figure 3 Vibratto Block Diagram

Vibratto Device Architecture

The Vibratto device architecture includes a RISC processor, CRT controller, transport mechanism, video encoder, memory controller, on-screen display (OSD) controller and video processor.

ESS RISC Processor

Embedded in the Vibratto is a 32-bit data pipelined RISC processor, with a combined 16 kb instruction and data cache subsystem. Programming of the RISC processor is done mostly in C. For applications involving an external host processor the communication between a host processor and the Vibratto is handled by a host interface module. The host interface can also be used for high speed data input and output.

The ESS RISC processor instruction and data cache subsystem is organized as a two-way set associative. On a cache load-miss and write-miss, the cache lines are allocated into the cache memory.

Before cache line operation, the writeback operation may be performed if the cache content and main memory contents are different. The ESS RISC also performs all power management and system configuration functions for the Vibratto, as shown in the block diagram in Figure 4.

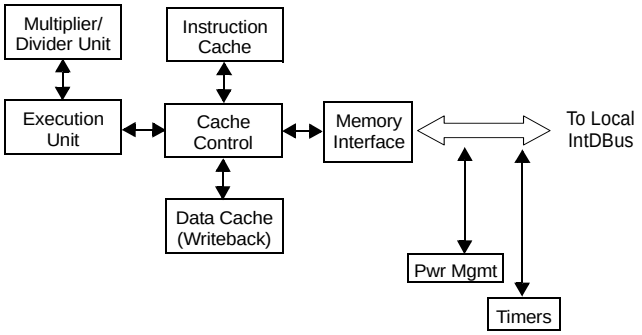


Figure 4 ESS RISC Block Diagram

The Programmable Multimedia Processor (PMP) core includes the proprietary single instruction, multiple data (SIMD) DSP, which can handle four 16-bit-wide data streams. Also included in the device architecture are a screen display controller, a digital video encoder with four DACs, a video input block, video system interfaces, FIFOs and DMA controllers. The PMP core resource can be accessed only from the ESS RISC core. Together, the ESS RISC and the PMP cores form ESS Technology's field-proven PMP engine.

Instruction Cache

The instruction cache of the RISC core is an on-chip memory array configured to a size of 8 kB. The cache is virtually indexed and physically tagged, allowing the virtual-to-physical address translation to occur in parallel with the cache access rather than having to wait for the physical address translation.

Data Cache

The data cache of the RISC core is an on-chip memory array configured to a size of 8 kB. Like the instruction cache, the data cache is also virtually indexed and physically tagged and handles the virtual-to-physical address translation process the same way as the instruction cache.

Table 2 lists the attributes for both the instruction and data caches of the Vibratto.

Table 2 Vibratto Instruction and Data Cache Attributes

Size	Set Associativity	Line Size	Write Policy
Instruction Cache			
8 kb	two-way set associative	16 bytes	N/A
Data Cache			
8 kb	two-way set associative	16 bytes	Writeback

RISC Interrupts

Twelve events can cause interrupts to the ESS RISC. Each event has a status bit to indicate the occurrence of the event and an enable bit to mask it from interrupting the ESS RISC. Table 3 lists all of the ESS RISC interrupts and the conditions that cause them.

Table 3 ESS RISC Interrupts

Interrupt	Group	Caused By Condition	How To Clear
Video IRQ	0	Video line number equals value in'videoirq'register	RISC EPROM and SRAM wait states
Timer	0	Timer register wraps from 3FFFFh to 00000h	Writing'1' to 'clrirq' register bit 3
BCDW	0	DMA Bus Controller Data is waiting to be read after DBUS-READ command	Reading the'rlatchl" register
Cmd Empty	0	DMA Bus Controller Command Queue goes empty	Writing a command to 'cmdque'
H En Idle	1	Huffman Encoder state machine goes idle	Writing '1' to 'clrirq' register bit 2
H De Idle	1	Huffman Decoder state machine goes idle	Writing '1' to 'clrirq' register bit 1
Data Transfer	1	Either Host-to-RISC Data TRE or RISC-to-Host DW (Host can select)	TRE cleared when RISC reads data; DW cleared when RISC writes data
Block Done	1	After DMA controller has read six blocks of RLAs from VP to DRAM	Write any data to 'clrhmade' register
Cmd Half-Empty	2	DMA Bus Controller Command Queue is less than or equal to half full	Write commands to 'cmdque' so queue becomes over half full
Debug	2	DEBUGIRQ pin goes high	DEBUGIRQ pin goes low
FIFO Level	2	Either Encoder Output FIFO or Decoder Input FIFO reach certain fullness	Writing '1' to bit 8 of 'mipctlreg' register
Host to RISC	2	Host sets Host-to-RISC interrupt bit 7 of 'HostControl0' register (Host address 2)	Writing'1' to bit 0 of'mipctlreg' register

Command Queue and Video Processor

Command Queue

The command queue module controls the video processor module of the RISC engine. The command queue allows the RISC to be decoupled from the video processor module by building a command list of instructions used to control its operation. The command list includes instructions for handling video processor DMA, data transfers, send and receive instructions, and waits to receive the current status of the video processor.

The depth of the command queue is approximately 64 entries. When the command queue is setting up DMAs for the video processor, the command queue automatically writes to DMA channel 0 of the Bus Controller.

The BUSCON_CMDQUE_VPDMASETUP register at index 0x20008200h accepts the video processor DMA access requests being routed to the command queue and prioritizes them in the respective order received. The incoming commands are always executed in the order they are written to the queue by the RISC. Both requests for 7-bit vales of delta-Y longwords (DELY[6:0]) and 9-bit values of delta-X scan lines (DELX[8:0]) are processed.

The BUSCON_CMDQUE_VPDMAADDR register at index 0x2000820Ch stores the DMA addresses of the incoming commands so that the command can be decoded when execution takes place.

The BUSCON_CMDQUE_STATUS register at index 0x20008224h constantly monitors the status of the command queue. The command queue of the Vibratto receives its DMA inputs from two of the three key bus controller registers.

Video Processor

The video processor consists of a programmable SIMD engine and 2 kb of internal cache memory. The video processor module performs instruction processing for four types of instructions:

- memory instructions
- conditional branch instructions
- compute instructions, and
- compute immediate instructions.

The video processor executes macroblock level tasks such as predictive coding, motion estimation, and motion compensation.

The video processor can also be used for a wide range of time-critical signal processing tasks, including Dolby Digital (AC-3) audio decoding and both video pre-processing and post-processing.

The video processor enables the Vibratto to perform arbitrary vertical filtering and scaling of outgoing video. The video processor is controlled by 32-bit and 16-bit wide dual issue micro-instructions. Commonly used microcode subroutines are stored in 8 kB of internal microcode ROM, while less frequently used microcode segments can be downloaded on demand to 2 kB of internal microcode RAM.

DMA Controller

The DMA bus controller is controlled by the video processor and controls multiple DMA channels for the transfer of 32-bit data between:

- video data bus and memory
- video decoder and memory
- ESS RISC and memory, and
- ESS RISC and video data bus.

Writes from the ESS RISC to the video processor command bus are also performed by the DMA bus controller, along with waits on status readback from the video processor status bus. A separate DMA channel is used for memory refresh. To improve memory bandwidth utilization, internal gateway FIFOs are used extensively.

The DMA controller includes two registers in the device architecture that interface directly to the video processor. The BUSCON_VP_CONTROL register at index 0x20008000h performs all video processor microcode loading and reset. The BUSCON_VP_STAT register at index 0x20008004h provides the status of the internal command queue of the video processor while monitoring the status of all sequencing, data transfers and I/O states.

Transport

The Vibratto incorporates a micro-programmable system demultiplexer capable of handling MPEG-1 system stream, MPEG-2 program stream, MPEG-2 transport stream, and other proprietary system multiplexes. The transport mechanism contains a 32-entry packet ID table and satisfies the transport requirements of the DVB standard.

The transport mechanism performs parsing of all packetized elementary streams (PESs) and selects the destinations for all of the audio and video elements in a given bit stream for processing by the ESS RISC engine. Each bit stream has a packet ID (PID) table, which includes a 4-bit destination field.

The transport mechanism determines the destination of the elements so that the ESS RISC engine knows where to send the final data output after processing. After processing, the transport mechanism also performs data flushing of all the buffer FIFOs in the device.

Private DMA Bus Interface

The Private DMA Bus interface of the Vibratto sets the priorities for handling data transfers. The Vibratto makes data transfers between the TDM interface the highest priority because devices connected to these interfaces, such as CD-ROM drives and DVD loaders, typically require specific timing for data transfers. Both CD-ROM drives and DVD loaders use the TDM interface as the physical path for data transfers between the drive/loader mechanism and the memory interface of the Vibratto.

Data transfers have intermediate priority because the resources that perform these data transfers are both internal to the Vibratto and have flexible timing requirements. Data transfers involving the host interface have the lowest priority in the Vibratto because host devices coupled to the host interface can be stalled if the data is not ready when requested. The Data Bus DMA is managed by the Bus Controller, while the Pribus DMA is managed by the transport mechanism. The Pribus DMA devices are listed in Table 4.

Table 4 Private Bus DMA Devices

Device Type	Application or Direction
Host	DRAM to Host
Decoder	Audio Decoder
	Video Decoder
Audio	Audio to DRAM (audio out)
	DRAM to Audio (audio in)
Video	Video to DRAM (video out)
	DRAM to Video (video in)
TDM	DRAM to TDM
Transport 1	Video bit stream to DRAM
Transport 2	Audio bit stream to DRAM
Transport 3	Aux1 to DRAM
Transport 4	Aux2 to DRAM

The Private Bus DMA ports are listed in Table 5.

Table 5 Private DMA Bus Ports

Gate Number	Application or Direction
Gate 1	Transport 1
Gate 2	Transport 2
Gate 3	Transport 3
Gate 4	Transport 4/Audio to DRAM
Gate 5	Audio decoder
Gate 6	Video decoder
Gate 7	DRAM to Audio
Gate 8	DRAM to TDM/DRAM to Host

The private bus DMA block diagram is depicted in Figure 5.

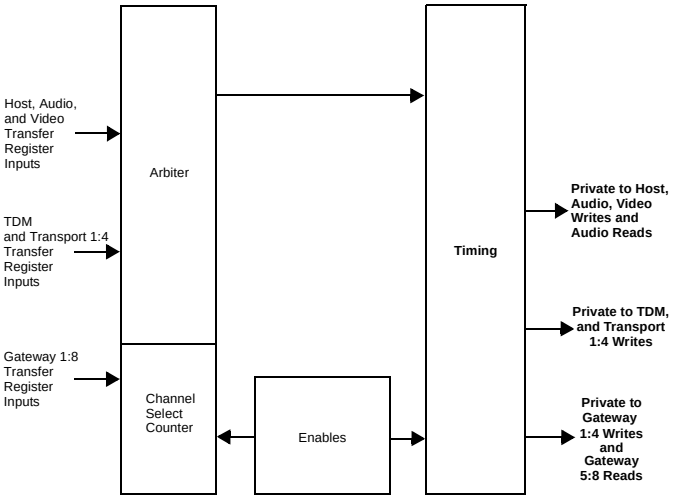


Figure 5 Private Bus DMA Block Diagram

Private Bus DMA Arbiter State Machine

The Vibratto includes a Private Bus DMA arbiter state machine. This state machine controls the read and write accesses to and from Pribus for all the devices within the Vibratto. The state machine receives all data waiting (DW) and transfer register empty (TRE) signals from the devices, and implements a round-robin dispatching scheme to drive enables to all the devices in the Vibratto.

Each of the four transport channels (video, audio, aux1 and aux2) will have a maximum latency of four CLK80 cycles. The maximum latency for all other transport channels are 16 CLK80 cycles each.

CRT Controller

The video output timing of the Vibratto is controlled by a pixel clock and the horizontal and vertical sync signals. Pixels are clocked out of the Vibratto by the pixel clock. The sync signals determine when the active video data is transferred. The timing of the active video and sync signals is determined by the CRT controller inside the Vibratto. The output timing can either be internally generated, or slaved to another video sync source.

Video Decoder

The Vibratto decoder module performs both MPEG-1 and MPEG-2 decoding and parsing. A high-speed engine decodes MPEG variable length codes (VLC), using built-in MPEG-1 and MPEG-2 VLC tables. A programmable RAM-based table controls automatic switching from one VLC table to the next.

The programmable table is primarily intended to allow JPEG images with custom Huffman tables to be decoded, but it also allows nonstandard codings to be decoded. The programmable table is also especially useful for H.261-compliant algorithms. Not only can H.261-based temporal coefficient (TCOEFF) tokens be decoded via the programmable table of the Vibratto, but so can Coded Block Pattern (CBP) tokens and motion vector tokens.

During decoding, the ESS RISC reads the incoming bitstream. The ESS RISC software determines the size and meaning of the token it is parsing and then discard the number of bits of the token. When the ESS RISC specifies incremental amount of the shift to be performed by writing to the applicable buffer, bits are shifted left out from the most significant end of the byte and new data from the buffer is shifted in at the least significant end.

The decoder is capable of operating in Block Mode and Step Mode. Regardless of the mode selected by the software, the decoder begins the decoding process with an intra-picture frame, or I-picture, which is transmitted to the decoder as a series of slices in a typical Group of Pictures (GOP).

Block Mode

In Block Mode, the decoder processes one of three different types of blocks:

- DC Luminance (Y) blocks
- DC Chrominance (UV) blocks
- AC blocks

The decoder decodes a specified number of macroblocks of data. The resulting Run Length Amplitude (RLA) tokens are written directly to the RLA output buffer. The decoder will decode up to six blocks of data and then go idle.

Step Mode

In Step Mode, a single token is decoded, rather than six tokens. The result can then be read by the ESS RISC instead of going to the applicable output buffer. After the decoder has processed the token, the decoder goes idle.

Video Encoder

The video encoder accepts digital linear CCIR601 YCbCr at square pixel data rates. Various color space conversion modes are provided to match the input data to the required output format. The data is then filtered to limit the bandwidth of the signals to within the supported ranges of the selected video standard.

The output of the encoder is fed directly into the output FIFO. The ESS RISC is also capable of writing variable length data into the FIFO in order to insert any non-TCOEFF parts into the bitstream. The RISC writes variable length data to the output FIFO up to 10 bits at a time. Smaller tokens can be written by right justifying fewer bits in the least significant bits of the data field. Since the output FIFO is shared between the ESS RISC and the encoder, the ESS RISC should only write to it when the encoder is idle

The encoder generates all the necessary synchronization signals for NTSC and PAL standards, which are inserted into the composite and luma outputs. Digital syncs are also provided for the rest of the system. The encoder also generates the corresponding sub-carrier frequency for color encoding. The encoder generates pixels at both square and nonsquare pixel data rates. This represents a pixel sampling rate of 13.5 MHz for both the NTSC and PAL video data streams.

These measurements assume internal 2x and 4x pixel data rate clock sources. Most of the processing is performed at a 2x pixel rate. The output rate is at a 4x pixel rate, which allows the output filtering to consist of a few passive components.

The encoder is a mixed digital/analog design which incorporates four 10-bit video DACs in the device architecture. This level of video DAC incorporation allows the Vibratto to generate composite, luma, and chroma outputs both in Y/C and YUV modes. The S-video luma and chroma outputs are summed internally to generate the composite video output in Y/C mode.

All filtering of the luminance and chrominance signals is performed using DSP techniques. The filters are programmable so that the encoder can provide enhanced bandwidth video for S-video output, but can also provide correctly band-limited signals for composite NTSC/PAL. The sync:white ratio is 40:100 IRE for both NTSC and PAL.

On-Screen Display (OSD) Controller

The 8-bit OSD controller provides display support for 256 palletized colors in eight degrees of transparency and can occupy the entire viewable area of a display or a portion of the display, depending on the system design. The OSD bitmap, which is stored in the reference memory, is multiplexed into the output video stream before color space conversion is performed.

The Vibratto performs its 3-bit blending of the on-screen display information when the LDMD bit (bit 2) of the VID_SCN_OSD_MISC register at index 0x20001124h is set, enabling bits 2:0 of the VID_SCN_OSD_PALETTE registers to establish the desired blending value for the different types of pixel modes required.

The settings of MODE bits 1:0 in the VID_SCN_OSD_MISC register determine the level of blending. Bits 3 of the VID_SCN_OSD_PALETTE registers enable the actual blending when set at 0. Modes

1 (2 bit/pixel), 2 (4 bits/pixel) and 3 (8-bit/pixel) are supported. For mode 3 (8-bit/pixel), the upper four bits of the pixel are the blend information, while the lower four bits of the pixel are the palette index and the blend information in the palette is ignored.

Subpicture Unit (SPU) Decoder

The Subpicture Unit (SPU) decoder separates and decodes the run-length subpicture pixel data stream and the corresponding subpicture commands that change the color and contrast values of each pixel type for different regions.

The output YUV of the SPU decoder is blended with the main video screen YUV values, depending on the contrast values. The SPU decoder supports four pixel types, coded 00, 01, 10, and 11. Each type represents a color (YUV) and contrast value (blending value with main picture).

The subpicture display area can also be divided into several horizontal stripes, each potentially with a different set of color/contrast values. Each stripe can be divided vertically into a maximum of 9 vertical regions (default 0, and changes 1-8), each region containing its own color/contrast value for each pixel type. In addition, there is a highlight feature that overrides all other color/contrast information for the SPU.

Main subpicture commands, such as SPU on/off, setting the size of the subpicture display area, default color and contrast, and the pointers to the color/contrast and pixel data are done by the ESS RISC engine. The ESS RISC sets the appropriate registers in the SPU, as well as the DMA channel for the command and data FIFOs, based on these commands.

SPU Video Data Framing

The SPU decoder receives its incoming video data in the data framing scheme depicted in Figure 6.

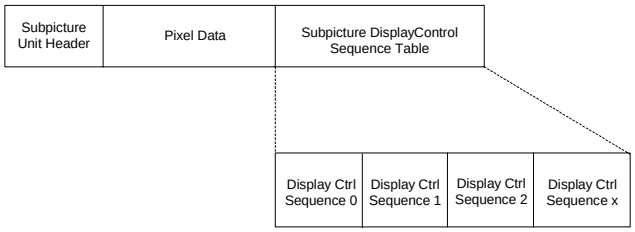


Figure 6 Typical Subpicture Data Framing Format

During decoding, the incoming SPU data packet is parsed for its pixel data and for its display control sequence information for decompression during video playback. If the last packet received by the SPU decoder is less than 2048 bytes, the packet will be stuffed with extra bytes as required.

Coding and Media Content Protection

The Vibratto supports a variety of captioning, coding and media content protection schemes that allow it to support media playback, regardless of the video encoding system used as the broadcast television standard for a specific country or geographic region.

NTSC Closed Captioning

The Vibratto supports the NTSC-compatible Line 21 captioning character set as required by EIA-608 and by FCC Part 15.119. The Vibratto displays the caption information during the blanked active line time of Line 21. The ASCII-based Line 21 character set appearing in Table 6 is the same as the one found in EIA-608 and in FCC Part 15.119.

Table 6 Line 21 Standard Character Set

Code	Symbol	Description
20		space
21	!	exclamation mark
22	“	quotation mark
23	#	number sign or pound sign
24	$	dollar sign
25	%	percent sign
26	&	ampersand
27	‘	apostrophe
28	(	open parenthesis
29	)	close parenthesis
2A	á	lowercase a with acute accent
2B	+	plus sing
2C	,	comma
2D	-	hyphen or minus sign
2E	.	period
2F	/	slash
30	0	zero
31	1	one
32	2	two
33	3	three
34	4	four
35	5	five
36	6	six
37	7	seven
38	8	eight
39	9	nine

Table 6 Line 21 Standard Character Set (Continued)

Code	Symbol	Description
3A	:	colon
3B	;	semicolon
3C	<	less-than sign
3D	=	equal sign
3E	>	greater-than sign
3F	?	question mark
40	@	at sign
41	A	uppercase A
42	B	uppercase B
43	C	uppercase C
44	D	uppercase D
45	E	uppercase E
46	F	uppercase F
47	G	uppercase G
48	H	uppercase H
49	I	uppercase I
4A	J	uppercase J
4B	K	uppercase K
4C	L	uppercase L
4D	M	uppercase M
4E	N	uppercase N
4F	O	uppercase O
50	P	uppercase P
51	Q	uppercase Q
52	R	uppercase R
53	S	uppercase S
54	T	uppercase T
55	U	uppercase U
56	V	uppercase V
57	W	uppercase W
58	X	uppercase X
59	Y	uppercase Y
5A	Z	uppercase Z
5B	[	open square bracket
5C	è	lowercase e with acute accent
5D	]	close square bracket
5E	ì	lowercase i with acute accent
5F	ò	lowercase o with acute accent
60	ù	lowercase u with acute accent
61	a	lowercase a
62	b	lowercase b
63	c	lowercase c

Table 6 Line 21 Standard Character Set (Continued)

Code	Symbol	Description
64	d	lowercase d
65	e	lowercase e
66	f	lowercase f
67	g	lowercase g
68	h	lowercase h
69	i	lowercase i
6A	j	lowercase j
6B	k	lowercase k
6C	l	lowercase l
6D	m	lowercase m
6E	n	lowercase n
6F	o	lowercase o
70	p	lowercase p
71	q	lowercase q
72	r	lowercase r
73	s	lowercase s
74	t	lowercase t
75	u	lowercase u
76	v	lowercase v
77	w	lowercase w
78	x	lowercase x
79	y	lowercase y
7A	z	lowercase z
7B	ç	lowercase c with cedilla
7C	÷	division sign
7D	Ñ	uppercase N-tilde
7E	ñ	lowercase n-tilde
7F		solid block

The Vibratto also detects the two-byte codes required by FCC Part 15.119 in the bitstream so that it can recognize the embedded captioning data that would otherwise go undetected during DVD playback. Each hex code shown in Table 7 is preceded by 11h for data channel 1 or by 19h for data channel 2. The Line 21 special character set appearing in Table 7 is the same as the one found in EIA-608 and in FCC Part 15.119.

Table 7 Line 21 Special Character Set

Hex	Example	Alternate	Description
30		See note[1]	Registered mark symbol
31	°		Degree sign
32	½		1/2 symbol
33	¿		Inverted (open) question mark (inverse query)
34	™	See note[1]	Trademark symbol
35	¢		Cents symbol
36	£		Pounds sterling
37	♪		Musical note
38	à		Lowercase a, grave accent
39			Transparent space
3A	è		Lowercase e, grave accent
3B	â		Lowercase a with circumflex
3C	ê		Lowercase e with circumflex
3D	î		Lowercase i with circumflex
3E	ô		Lowercase o with circumflex
3F	û		Lowercase u with circumflex

[1]**NOTE:** The registered and trademark symbols are used to satisfy certain legal requirements. There are various legal ways in which these symbols may be drawn or displayed. For example, the trademark symbol may be drawn with the “T” next to the “M” or over the “M.” It is preferred that the trademark symbol be superscripted, i.e., XYZ™. It is left to each individual manufacturer to interpret these symbols in any way that meets the legal needs of the user.

PAL Teletext Captioning

The Vibratto supports teletext insertion and captioning typically used in the PAL system. During teletext insertion, pages of text are transmitted as digital information along with the normal television signal from the video FIFOs of the Vibratto during the blanking interval. The scan lines which are sent after the scan lines for picture sync contain the teletext data.

CPPM, CSS-2, and Macrovision

The Vibratto implements CPPM- and CSS2-compliant digital content protection for prerecorded audio and video media. For additional analog content protection of prerecorded media, the Vibratto also supports the Macrovision anti-copy process.

AC-3 Audio Decoding (NTSC)

The AC-3 audio format is used in the NTSC television format, while the MPEG-2 audio format is used in the PAL television format. An AC-3 serial coded audio bitstream is comprised of a sequence of sync frames, with each frame representing 256 new audio samples, as shown in Figure 7.

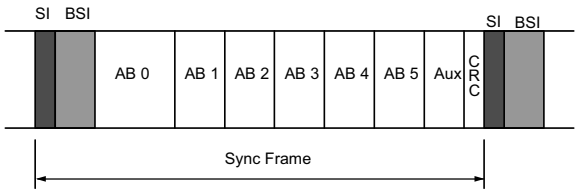


Figure 7 Typical AC-3 Sync Audio Framing

As required by Standard A/52 of the Advanced Television Systems Committee (ATSC), the beginning of each frame starts with the Sync Information (SI) header, followed by the Bit Stream Information (BSI) header and Audio Blocks (AB) 0 through 5.

The audio blocks may be followed by an auxiliary (Aux) data field. At the end of each frame is an error check field that includes a CRC word for error detection. An optional CRC word may also be added in the SI header, if desired, for greater accuracy and enhanced error detection in the decoding process.

During AC-3 decoding, the compressed AC-3 data is input into the Vibratto at 384 kb/s, and contains 5.1 channels of audio data. The five channels represent five full-frequency range channels of stereo audio data, while the.1 channel represents one low frequency effects (LFE) channel of audio data, usually processed as subwoofer-type audio.

Once the audio is decompressed into its native 5.1 channel format, the audio data can be sent directly to the speakers only if the DVD player has the required number of speakers for each channel. If the DVD player does not have the required number of speakers, the Vibratto will downmix the six channels of audio data into fewer channels automatically.

AC-3 Encoding (NTSC)

During AC-3 encoding, the Vibratto accepts up to 24-bit PCM words of audio. The Vibratto locks the input sample rate to the output bit rate so that each AC-3 sync frame contains 1536 samples of audio (1536 samples ÷ 6 frames = 256 samples per frame). If the input audio is available in PCM format at a different sample rate than required, the Vibratto performs sample rate conversion to conform to the AC-3 sampling rate before frame packing occurs.

The Vibratto performs high-pass filtering on the individual full-frequency input channels and removes any DC components of signals in order to allow more efficient coding to occur, while the LFE channel is low-pass filtered.

The Vibratto forms the coupling channel by adding all of the individual channel coefficients together and dividing the sum by 8. Dividing the sum of the coefficients prevents the coupling channel from exceeding a value of 1. The Vibratto determines which coefficients are to be quantized to zero and reproduced with dither on a per channel basis. When the Vibratto packs the bit stream into the encoded AC-3 frame, the frame may be output in a burst or delivered as a serial data stream at a constant rate.

DTS Multi-Channel Decoding

The Vibratto supports DTS multi-channel decoding for both audio CD and DVD media playback. The Vibratto supports audio post-processing, including bass management. Separate downloads can be used to support stereo to 5.1 channel effects processing. The DTS 6-channel decoder operates in real time and allows the channels to be monitored through the decoding cycle. The compressed data output is on a single AES-EBU channel and is clocked synchronously by the digital audio inputs.

The decoding does not involve calculations that are of importance to the quality of the decoded audio. After synchronization, the decoder unpacks the compressed audio bitstream, detects and corrects any transmission-induced errors and demultiplexes the data into individual audio channels.

DVD-Audio (ES6038 Only) and MLP Decoding

The Vibratto implements Meridian Lossless Packing (MLP) decoding in order to support high-end audio features such as DVD-Audio. During MLP decoding, up to 63 channels of 24-bit audio can be sampled at rates as high as 192 kHz. The use of sampling rates this high allows the ES6038 to support multichannel audio applications such as 6-channel DVD-Audio.

MLP Decoding

During MLP decoding, the Vibratto manipulates each encoding process in reverse order. Incoming channels are losslessly matrixed into a number of separate substreams in order for it to access a subset of the overall signal.

The incoming MLP bitstreams carry all the information necessary for decoding, including instructions to the decoder, the compressed data itself, lossless testing information and CRC check data. After the Vibratto de-interleaves the bitstream and extracts the decoding parameters from the bitstream headers, entropy decoding is performed. The inter-channel correlations that were stripped out during the encoding process are re-established during decoding. When the bitstream is losslessly matrixed, the bitstream is successfully decoded for playback.

MLP Encoding

During MLP encoding, the Vibratto takes advantage of the FIFOs and various filters in the device architecture to manage the data buffering process efficiently while also ensuring the decoding process remains lossless. The Vibratto detects those channels that do not use all of the available bandwidth and strips out any unnecessary inter-channel correlations using entropy coding, lossless processing and lossless matrixing. These three processes reduce the instantaneous peak data rate for best results during data sampling.

HDCD Decoding and Filtering

The Vibratto performs HDCD-compliant decoding using its interpolation filtering capabilities during playback of HDCD-encoded media in audio CD, DVD and Video CD modes. Decoding of HDCD-encoded media occurs automatically in the Vibratto when HDCD process information is detected in the audio input data.

The HDCD implementation in the Vibratto is primarily oriented towards the industry standard CD–Digital Audio (CD-DA) format, defined in the Red Book. The Vibratto supports HDCD precision filtering for HDCD- and non-HDCD-encoded audio bitstreams alike. Both 1x and 2x filtering methods are also supported.

HDCD code is similar to the packet type of data sent in the Ethernet network protocol in that the bitstreams include the use of descriptors. During quantization, the packet of HDCD code is inserted into the LSB of the 16-bit audio word during encoding of the CD/DVD media. The Vibratto reduces the decoded average signal level of the HDCD process information in the audio input, allowing increased overhead for the expanded dynamic range.

Progressive Scan (ES6028 and ES6038 Only)

The ES6028 and ES6038 both support the progressive scan reconstruction process as well as interlaced video for the NTSC and PAL formats during DVD playback. The ES6028 and ES6038 support both baseline and progressive JPEG decoding. Due to the limitation of memory, the Vibratto software supports only a limited size JPEG picture. Baseline pictures having more than 5120x3840 resolution, and progressive scan pictures having more than 2048x1536 resolution are not currently supported.

In order to show a progressive image, the CRT controllers of both the ES6028 and ES6038 are driven to generate and refresh the scan lines used to create the active display at a rate double that of the refresh speed used by the NTSC system. Because the CRT controllers of the ES6028 and ES6038 are driving the CRT circuitry of the external video monitor to scan and refresh the active display at twice the speed, both can draw an entire frame in the same amount of time it takes to draw a single field.

The progressive scan features of the ES6028 and ES6038 make the faster screen refresh possible, allowing for a flicker-free picture of superior quality to be displayed during DVD playback, while also reducing the number of scan lines visible to the unaided eye. The ES6038 is actually faster because the processing overhead used for DVD-Audio in the other Vibratto devices is instead available for progressive scan operations.

Unlike interlaced video, every scan line of a complex video frame is refreshed when using progressive scan. Since the reconstruction process of de-interlaced video is a digital process, the reconstruction process is a lossless one during A/D and D/A conversion of the bitstream.

Video Error Concealment

The MPEG decoder handles bitstream errors while performing video error concealment during DVD and VCD/SVCD playback. The Vibratto processors all support three modes of video error concealment presented in Table 8:

Table 8 Video Error Concealment Modes

Mode	Type	Description
0	Adaptive	Automatically switches the Vibratto between the blocky and jerky modes.
1	Jerky	Show good pictures, but not smoothly.
2	Blocky	Shows pictures smoother, but in more of a blocky fashion.

Disk Error Concealment

When a read error occurs during DVD playback, video object units (VOBUs) are skipped by the Vibratto. If the number of VOBUs to be skipped exceeds the range of the available data, the Vibratto skips some sectors on the media until the presence of a new error correction control block is detected in the bitstream.

Device Interfaces

Audio Interface

The audio interface is a bidirectional serial port that connects to an external audio ADC/DAC for the transfer of PCM (pulse coded modulation) audio data in I²S format. It supports 16-, 24-, and 32-bit audio frames. No external master clock is required. The Vibratto offers two audio interface modes:

1. Stereo mode using TSD0 on pin 33.
2. Dolby™ Digital (AC-3) and DTS 5.1 channel mode using TSD[2:0] on pins [37:36, 33]

The Vibratto audio mode configuration is selectable, allowing it to interface directly with low-cost audio DACs and ADCs. The audio port provides a standard I²S interface input and output and S/PDIF (IEC958) audio output. Stereo mode is in I²S format while six channel Dolby™ Digital and DTS (5.1 channel) audio output can be channeled through the I²S interface and S/PDIF.

The S/PDIF interface consists of a bi-phase mark encoder, which has low skew. The transmit I²S interface supports the 128, 192, 256, 384, and 512 sampling frequency formats, where sampling frequency Fs is usually 32 kHz, 44.1 kHz, 48 kHz, 96 kHz, or 192 kHz. The audio samples for the I²S transmit interface can be 16, 18, 20, 24, and 32-bit samples.

For Linear PCM audio stream format, the Vibratto supports 48 kHz and 96 kHz. Dolby Digital and DTS audio only supports 48 kHz. The Vibratto incorporates a built-in programmable analog PLL in the device architecture in order to generate a master audio clock.

The MCLK pin is for the audio DAC clock and can either be an output from or an input to the Vibratto. Audio data out (TSD) and audio frame sync (TWS) are clocked out of the Vibratto based on the audio transmit bit clock (TBCK). Audio receive bit clock (RBCK) is used to clock in audio data in (RSD) and audio receive frame sync (RWS).

DVD Loader Interfaces

The Vibratto supports the AT Attachment Packet Interface (ATAPI), DVD Control Interface (DCI), Integrated Drive Electronics (IDE), and Universal Drive Format (UDF) parallel and serial port interfaces used by many types of DVD loaders. These interfaces meet the specification of many DVD loader manufacturers.

ATA/IDE Loader Interface

The host interface can directly support ATAPI devices such as DVD drives or I/O controllers. PIO modes 0 through 4 are supported. The ATA/IDE interface can directly control two devices through the use of the HCS1FX# and HCS3FX# signals. The ATA/IDE interface of the Vibratto uses a command execution protocol that allows the operation of audio-CD and DVD loaders to coexist on the same type of interface cable that most computers use for CD loaders and hard disk drives.

Table 9 lists the packet commands and the respective command codes for ATAPI C/DVD devices as specified by SFF-8090i.

Table 9 Packet Commands for ATAPI C/DVD Devices

Code	Command Name
00h	TEST UNIT READY
03h	REQUEST SENSE
04h	FORMAT UNIT
12h	INQUIRY
1Bh	START/STOP UNIT
1Eh	PREVENT/ALLOW MEDIUM REMOVAL
23h	READ FORMAT CAPACITIES
25h	READ CAPACITY
28h	READ (10)
2Ah	WRITE (10)
2Bh	SEEK
2Eh	WRITE AND VERIFY (10)
2Fh	VERIFY (10)
35h	SYNCHRONIZE CACHE
42h	READ SUBCHANNEL
43h	READ TOC/PMA/ATIP
44h	READ HEADER
45h	PLAY AUDIO (10)
46h	GET CONFIGURATION
47h	PLAY AUDIO MSF
4Ah	GET EVENT/STATUS NOTIFICATION
4Bh	PAUSE/RESUME
4Eh	STOP PLAY/SCAN
51h	READ DISC INFORMATION
52h	READ TRACK/RZONE INFORMATION
53h	RESERVE TRACK/RZONE
54h	SEND OPC INFORMATION
55h	MODE SELECT (10)
58h	REPAIR RZONE
5Ah	MODE SENSE (10)
5Bh	CLOSE TRACK/RZONE/SESSION/BORDER
5Dh	SEND CUE SHEET
A1h	BLANK
A2h	SEND EVENT
A3h	SEND KEY
A4h	REPORT KEY
A6h	LOAD/UNLOAD MEDIUM

Table 9 Packet Commands for ATAPI C/DVD Devices

A7h	SET READ AHEAD
A8h	READ (12)
AAh	WRITE (12)
ACh	GET PERFORMANCE
ADh	READ DVD STRUCTURE
B6h	SET STREAMING
B9h	READ CD MSF
BAh	SCAN
BBh	SET CD SPEED
BCh	PLAY CD
BDh	MECHANISM STATUS
BEh	READ CD
BFh	SEND DVD STRUCTURE

Compact Flash Interface

The Vibratto provides True IDE Mode firmware support for the Compact Flash storage card interface found on a variety of removable storage cards used by digital cameras and on MP3 players.

By implementing Compact Flash support, the Vibratto can readily detect the insertion and removal of a Compact Flash card, which also constitutes a hot-swapping event. During a hot-swapping event, the CARD_DETECT signal is asserted by the Vibratto, allowing it to determine the presence of the removable storage card fully inserted into its socket.

The Vibratto permits both 8- and 16-bit common memory I/O accesses with a removable storage card via the host interface. Table 10 lists the CF-ATA command set.

Table 10 CF-ATA Command Set

Class	Command	Code
1	CHECK POWER MODE	E5h or 98h
1	EXECUTE DRIVE DIAGNOSTIC	90h
1	ERASE SECTOR(S)	C0h
1	IDENTIFY DRIVE	ECh
1	IDLE	E3h or 97h
1	IDLE IMMEDIATE	E1h or 95h
1	INITIALIZE DRIVE PARAMETERS	91h
1	READ BUFFER	E4h
1	READ LONG SECTOR	22h or 23h
1	READ MULTIPLE	E4h
1	READ SECTOR(S)	20h or 21h
1	READ VERIFY SECTOR(S)	40h or 41h
1	RECALIBRATE	1Xh
1	REQUEST SENSE	03h
1	SECURITY DISABLE PASSWORD	F6h
1	SECURITY ERASE PREPARE	F3h
1	SECURITY ERASE UNIT	F4h
1	SECURITY FREEZE LOCK	F5h
1	SECURITY SET PASSWORD	F1h
1	SECURITY UNLOCK	F2h

Table 10 CF-ATA Command Set (Continued)

Class	Command	Code
1	SEEK	7Xh
1	SET FEATURES	EFh
1	SET MULTIPLE MODE	C6h
1	SET SLEEP MODE	E6h or 99h
1	STAND BY	E2h or 96h
1	STAND BY IMMEDIATE	E0h or 94h
1	TRANSLATE SECTOR	87h
1	WEAR LEVEL	F5h
2	FORMAT TRACK	50h
2	WRITE BUFFER	E8h
2	WRITE SECTOR(S)	30h or 31h
2	WRITE LONG SECTOR	32h or 33h
2	WRITE SECTOR(S) W/O ERASE	38h
3	WRITE VERIFY	3Ch
3	WRITE MULTIPLE	C5h
3	WRITE MULTIPLE W/O ERASE	CDh

DVD Control (DCI) Loader Interface

The DCI interface routes incoming DVD bitstreams from the DCI loader to the Vibratto via the DVD descrambler so that the DVD bitstreams can be decoded for decompression and playback. DCI_FDS# indicates the beginning of each sector on the DVD medium. The DCI_ERR# signal indicates the error per data byte. DCI_ACK# indicates an acknowledge signal from the servo that a data byte is ready to be transferred. The DCI_REQ# line is used by the Vibratto to inform the servo that it is ready to receive data.

Universal Disk Format (UDF) Loader Interface

The UDF 2.01 loader interface routes incoming DVD bitstreams from a UDF loader, typically a CD-R or DVD-R loader, to the Vibratto via the DVD descrambler so that the DVD bitstreams can be decoded for decompression and playback. The UDF entity identifier definitions are listed in Table 11.

Table 11 UDF Entity Identifier Definitions

Entity Identifier	Description
OSTA UDF Compliant	Contents of the specified volume comply with domain specified by the UDF Specification.
UDF LV Info	Contains additional logical volume information.
UDF FreeAppEASpace	Contains free unused space within the application extended attributes space.
UDF DVDCGMS Info	Contains DVD Copyright Management Information.
UDF Virtual Partition	Describes UDF Virtual Partition.
UDF Sparable Partition	Describes UDF Sparable Partition.
UDF Sparing Table	Contains information for handling defective areas on the media.

Host Interface

The host interface of the Vibratto allows communication between the RISC and an external host, and is comprised of three ports. Two of these ports are the 8-bit wide debug and command ports, with the third being the 16-bit wide DMA port. The command port transfers control and status information between the host and the Vibratto. The external host controls the Vibratto through the command port.

The debug port provides a path to the RISC core for debugging purposes. This allows programmers access to the state of the hardware and the software without disturbing the command or DMA ports.

The DMA port transfers data to be multiplexed with the audio and video data in an encoded bitstream. This mechanism allows applications such as file transfers to occur. Additionally, the DMA port can carry both the audio and the encoded bitstream.

The host interface has two registers that control the operation of the flags and interrupts, R_HOSTRQSTAT and R_HOSTMASK for the RISC side and H_HOSTRQSTAT and H_HOSTMASK for the host side. Flags indicate the readiness of the Vibratto to accept or supply data over the host interface DMA channel. Interrupts may be used for exception indication from RISC-to-host or from host-to-RISC. The interrupts are maskable.

The pulse width high times of the HRDREQ# and HWRREQ# signals are defined as minimum values only. The maximum values of these parameters are software dependent. The internal DMA channel bandwidth depends upon the presence of other DMA operations in the Vibratto.

System SRAM Interface

The system SRAM interface controls access to optional external SRAM which can be used for RISC code, stack, and data. The SRAM bus supports four independent address spaces, each having programmable bus width and wait states. The interface can support not only SRAM but also ROM/EPROM and memory-mapped I/O ports for standalone applications.

The Vibratto inserts from 1 to 32 wait states into each cycle, with each wait state being one clock cycle long. RISC accesses can involve just one wait state. When switching from a low speed bank to a high speed bank, the turnoff delay of the low speed bank can overlap the first access of the high speed bank. To prevent data corruption, bank select delay time t_{BS_DT} is programmable for each SRAM bank from 0 to 3T states.

The signals for the SRAM bus are generated from the internal RISC clock and are timed in integer multiples of clock cycles, except for the write strobe, which is delayed by one-half cycle from the address setup and advanced one-half cycle from the start of the next access cycle. The SRAM interface signal skew may vary with the Vibratto speed grade.

TDM Interface

The Vibratto implements a high-speed, bidirectional serial bus known as a TDM interface that supports a number of high-speed serial protocols. The TDM interface can also act as a general-purpose 16-Mbps serial link when not constrained by TDM protocols.

The TDM interface provides an easy connection between the Vibratto and available communications chips. The TDM interface is a time-division-multiplexed bus that multiplexes byte data on up to 64 channels. Time slot 0 starts after N (which can be set in the XMT/RCVDELAY register) clocks after the frame starts. Each slot is eight clock periods long, and either transmits or receives byte data during a write cycle or a read cycle. Immediately after slot 0 completes, slot 1 starts and so on.

Each channel is allocated a different time slot on the bus, and the Vibratto can be set to send and receive data in any combination of different time slots. Data is assumed to be ordered by time slot; e.g., if time slots 6, 8, and 17 are used, the first DMA byte sent to memory would be in time slot 6, followed by time slots 8 and 17 in order. Reordering must be done in software.

The interface consists of frame sync signal TDMFS, data transmit and receive signals TDMDX and TDMDR, external buffer enable signal TDMTSC# and bit clock signal TDMCLK. The timing of the data transfer is externally controlled. The TDM interface can support a number of different timings. The TDM interface supports both Forms 1 and 2 of the XA Mode format as required by ISO 9660.

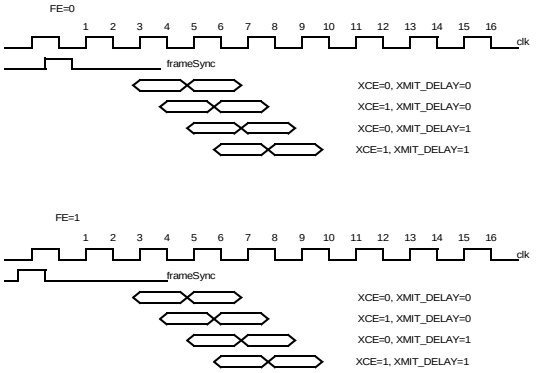
The TDM interface can transfer data at a maximum rate of 16 Mbps, with a more typical configuration supporting a data rate of up to 4.096 Mbps with a frame sync frequency of 8 kHz. The TDM interface hardware is flexible enough to interface with a wide range of communications chips for ISDN, PABX, LAN and WAN connectivity.

The Vibratto interfaces especially well with those devices that support the concentration highway interface (CHI) bus, ISDN-oriented modular revision 2 (IOM-2) interface, and multi-vendor integration protocol (MVIP).

The TDM interface programmability includes independent receive, transmit, and frame sync clock edge selection and independent receive and transmit data offsets.

TDM Operation and Bit Settings

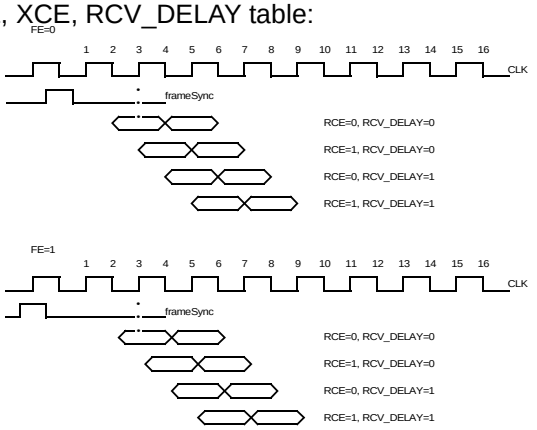
1. To turn on the TDM, set the tdm_rst bit (bit 5) in the TDMCTL0 register to 0, then to 1.
2. To reset the TDM internal registers, set tdm_tstbit (bit 10) in the TDMCTL0 register to 1, then to 0.
3. The slot registers must be set, there are no default values.
4. When using 2x clock, the crefphase bit has to be set and the p bit in the XMT/RCVDELAY register must be 0.
5. When using 2x clock, the values in tables must be multiplied by 2.
6. FE, XCE, XMT_DELAY table:



XMT_DELAY

FE	XCE	0	1	2	3	4	5	6	7	Note
0	0	3	5	7	9	11	13	15	17	start x-mit on rising
0	1	4	6	8	10	12	14	16	18	start x-mit on falling
1	0	3	5	7	9	11	13	15	17	start x-mit on falling
1	1	4	6	8	10	12	14	16	18	start x-mit on rising

7. FE, XCE, RCV_DELAY table:



		RCV_DELAY								
FE	RCE	0	1	2	3	4	5	6	7	Note
0	0	4	6	8	10	12	14	16	18	sampled on falling
?	1	3	5	7	9	11	13	15	17	sampled on rising
?	0	4	6	8	10	12	14	16	18	sampled on rising
?	1	3	5	7	9	11	13	15	17	sampled on falling

Vacuum Fluorescent Display (VFD) Interface

The Vibratto provides hardware support for the vacuum fluorescent display (VFD) interface in DVD player designs. The VFD_CTRL register at index 0x200013CCh is programmed by the software for supporting the control and format functions in the first access, and enables the interface in the second access.

The VFD_DATA register at index 0x200013D0h, along with the AUX_MODE register at index 0x20001340h both act as containers for an external VFD device to read data from it and write VFD clock and data to it during normal operations. The SYS_STATUS register at index 0x200013D8h and the IR_DIFF register at index 0x200013DCh provide additional hardware support for remote control operations.

Video Memory Interface

The Vibratto provides a glueless 16-bit interface to DRAM memory devices used as video memory for a DVD player. The maximum amount of memory supported is 16 MB of Synchronous DRAM (SDRAM). The memory interface is configurable in depth to support 128-Mb addressing.

The memory bus interface generates all the control signals to interface with external memory. The Vibratto supports different configurations using the memory configuration bits SDCFG[1:0] (bits 12:11), the SD8BIT bit (bit 14), and SD64M bit (bit 15) in the BUSCON_DRAM_CONTROL register located at index 0x20008100h. Configurations can be implemented in many ways. Table 12 lists the typical SDRAM configurations used by the Vibratto.

Table 12 Typical SDRAM Configurations

Size (MB)	Bit Order				Memory Configuration
	SD64M	SD8BIT	SDCFG1	SDCFG0	
2.0	0	0	0	1	1 pc: 512Kx16x2 (16 Mb)
4.0	0	0	0	0	2 pcs: 512Kx16x2 (16 Mb)
4.0	0	1	0	1	2 pcs: 1Mx8x2 (16 Mb)
8.0	0	1	0	0	4 pcs: 1Mx8x2 (16 Mb)
8.0	1	0	X	X	1 pc: 1Mx16x4 (64 Mb)
16.0	1	0	X	X	2 pc: 1Mx16x4 (64 Mb)
16.0	1	1	X	X	2 pc: 2Mx8x4 (64 Mb)
16.0	1	1	X	X	1 pc: 2Mx16x4 (128 Mb)

The memory interface controls access to both external SDRAM or EDO memories, which can be the sole unified external read/write memory acting as program and data memory as well as various decoding and display buffers. At high clock speeds, the Vibratto memory bus interface has sufficient bandwidth to support the decoding and displaying of CCIR601 resolution images at full frame rate.

SDRAM Considerations

The Vibratto uses SDRAM with a programmed CAS# latency of three clocks (CL=3) and sequential burst of full page length. Performance based on SDRAM is double that of EDO. SDRAM must be software configured before any memory access. The programmable SDRAM refresh period can be modified to meet any desired configuration.

SDRAM Address Mapping

The memory address (LA) is mapped to the DMA address, which is formed by ADDR in the BUSCON_DMA_ADDR registers. The result is then converted into the DRAM control signals using the SDCFG[1:0] configuration bits (bits 12:11) and the SD8BIT bit (bit 14) in the BUSCON_DMA_CONTROL register located at index 0x20008100h.

SDRAM Configuration Requirements

Table 13 shows SDRAM memory size configurations, each with its corresponding signal pins.

Table 13 SDRAM Configurations and Signal Pins

Size (MB)	SDRAM 0	SDRAM 1	SDRAM2	SDRAM3	Memory Type
2.0	DCAS# DRAS0# DCS0# DB[0:15]				512Kx16x2 (16 Mb)
4.0	DCAS# DRAS0# DCS0# DB[0:15]	DCAS# DRAS0# DCS1# DB[0:15]			512Kx16x2 (16 Mb)
4.0	DCAS# DRAS0# DCS0# DB[0:7]	DCAS# DRAS0# DCS1# DB[8:15]			1Mx8x2 (16 Mb)
8.0	DCAS# DRAS0# DCS0# DB[0:7]	DCAS# DRAS0# DCS0# DB[8:15]	DCAS# DRAS0# DCS1# DB[0:7]	DCAS# DRAS0# DCS1# DB[8:15]	1Mx8x2 (16 Mb)
8.0	DCAS# DRAS0# DCS0# DB[0:15]				1Mx16x4 (64 Mb)
16.0	DCAS# DRAS0# DCS0# DB[0:15]	DCAS# DRAS0# DCS1# DB[0:15]			1Mx16x4 (64 Mb)

Table 13 SDRAM Configurations and Signal Pins

Size (MB)	SDRAM 0	SDRAM 1	SDRAM2	SDRAM3	Memory Type
16.0	DCAS# DRAS0# DCS0# DB[0:7]	DCAS# DRAS0# DCS0# DB[8:15]			2Mx8x4 (64 Mb)
16.0	DCAS# DRAS0# DCS0# DB[0:15]				2Mx16x4 (128 Mb)

Video Interface

Video Display Output

The video output section controls the transfer of video frames stored in memory to the internal TV encoder of the Vibratto. The output section consists of a programmable CRT controller capable of operating either in Master or Slave mode. Figure 8 shows the display timing on the screen.

The video output section features display FIFOs to buffer outgoing luminance and chrominance data while also performing YUV4:2:0 to YUV4:2:2 conversion. Arbitrary horizontal decimation and interpolation is achieved by a polyphase filter. Together with programmable line dropping/duplication circuitry and micro-code based post-processing running on the video processor, the Vibratto is capable of arbitrating image conversion. Examples include SIF to CCIR601, letter-box, NTSC to PAL, and PAL to NTSC conversions.

Video Bus

The Vibratto video bus transfers digital video pixels out of the chip. In standalone applications the video bus will be connected to a monitor or an LCD panel. In workstation applications, the output bus will feed an overlay circuit so that the output video appears in a window of the Graphical User Interface (GUI).

The video bus has 8 YUV data pins that transfer luminance and chrominance (YUV) pixels in CCIR601 pixel format (4:2:2). In this format, there are half as many chrominance (U or V) pixels per line as luminance (Y) pixels; there are as many chrominance lines as luminance.

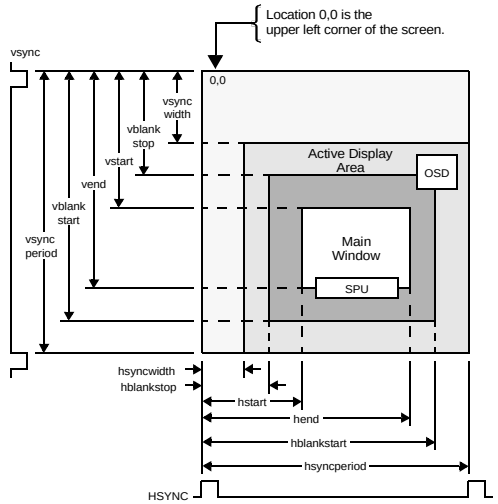


Figure 8 Video Output Timing

Safe Caption Area

The Vibratto draws the safe caption area required by FCC Part 15.119 as shown in Figure 7.

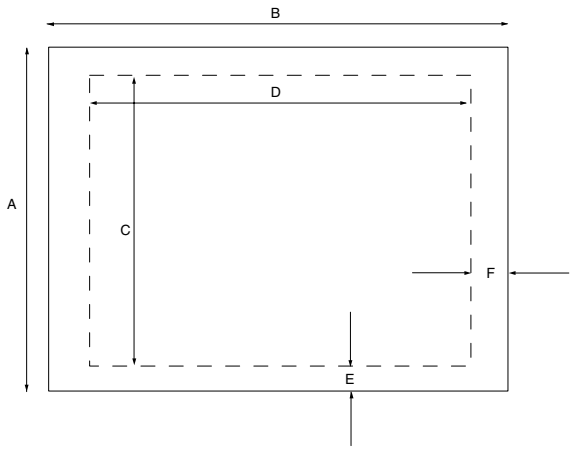


Figure 9 Safe Caption Area

The dimensions of the safe caption area are listed in Table 14.

Table 14 Safe Caption Area Dimensions

Label	Dimension	Percent of Picture Height
A	Television picture height	100.0
B	Television picture width	133.33
C	Height of safe caption area	80.0
D	Width of safe caption area	106.67
E	Vertical portion of safe caption area	10.0
F	Horizontal portion of safe caption area	13.33

Video Post-Processing

The Vibratto video post-processing circuitry provides support for the color conversion, scaling, and filtering functions through a combination of special hardware and software. Horizontal up-sampling and filtering is done with a programmable, 7-tap polyphase filter bank for accurate non-integer interpolations. Vertical scaling is achieved by repeating and dropping lines in accordance with the applicable scaling ratio. Figure 10 shows the video post-processing functional blocks. The first two processing steps are performed by the video processor core. Video post-processing can be applied on the decoded images to improve the picture quality.

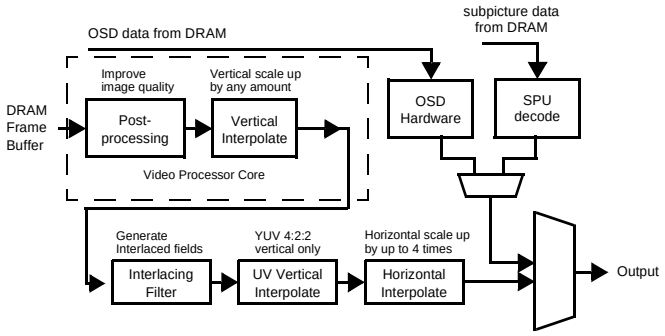


Figure 10 Video Post-Processing

The next stage in the processing, applicable only to low resolution MPEG-1 video, is an interlacing filter that generates even and odd fields from decoded frames for applications that use a TV screen. The filter improves both the spatial and temporal appearance of the decoded images on interlaced displays. Following the interlacing filter is an interpolation section that uses bilinear interpolation to increase the resolution of the chrominance components by a factor of two in the vertical dimension. This interpolation section converts from the MPEG chrominance subsampling to that used by CCIR601. The resulting YUV pixels can then be passed through a 7-tap horizontal interpolation filter that increases the horizontal resolution of the image by up to four times. The horizontal filter automatically chooses between five sets of filter coefficients based on the fractional component of the new position of the pixel in the video data stream. The filter coefficients are 8 bits wide. The filter length is selectable as 1, 3, 5, or 7 taps. The relationship between PCLK2XSCN and internal RISC clock is shown in Table 15.

Table 15 ESS RISC Clock Relationship to Pixel Clocks

Taps	Restrictions	Frequency
3	Pixel rate < (Internal RISC CLK)/2	27 MHz
5	Pixel rate < (Internal RISC CLK)/3	20 MHz
7	Pixel rate < (Internal RISC CLK)/4	default 13.5 MHz

Video Timing

The video bus can be clocked either by double pixel clock and clock qualifier or by a single pixel clock. The double clock typically is used for TV displays, the single for computer displays. PCLKQSCN is ignored in 1x clock mode. The timing of the syncs and odd/even field indication is shown in Figure 12 and Figure 13. The output video field indication is done by modifying the relative positions of VSYNC and HSYNC. At the start of an even field, the horizontal and vertical sync pulses will start on the same clock edge; in odd fields the horizontal sync pulse will be delayed by one clock cycle. The polarity of both horizontal and vertical syncs is programmable.

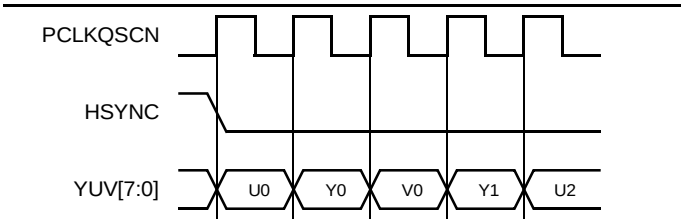


Figure 11 8-bit YUV Input Timing

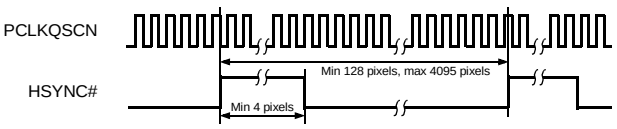


Figure 12 Horizontal Video Timing

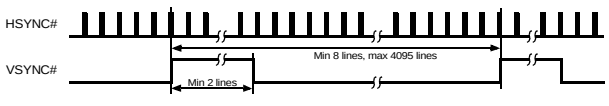


Figure 13 Vertical Video Timing

REGISTERS

Host Interface (Host Side) Registers

This section describes the host interface (host side) registers of the Vibratto.

H_HOSTDMAPORT (0x0, R/W)

Host Interface (DMA Port) Data
15:0

The Host Interface DMA Port register contains memory and I/O data transferred to and from the RISC. After reset, it is initialized to 0x0000.

H_HOSTVCXPORT (0x1, R/W)

Host Interface (Command Port) Data
7:0

The Host Interface Command Port register contains control and status data transferred to and from the RISC. After reset, it is initialized to 0x00.

H_HOSTDBGPORT (0x2, R/W)

Host Interface (Debug Port) Data
7:0

The Host Interface Debug Port register transfers data to and from the RISC during debugging. After reset, it is initialized to 0x00.

H_HOSTCTL (0x3, R/W)

H2R_IRQ	ISEL	OSEL	CLR_RIRQ
7	6:4	3:1	0

The Host Interface Control register enables and disables the host-to-RISC and RISC-to-host interrupt capabilities of the UP68D01-2811. After reset, it is initialized to 0x00.

Bits	Name	Description
7	H2R_IRQ	Host to RISC IRQ Enable. Writing a 1 to this bit sets the host to RISC IRQ flag.
6:4	OSEL [2:0]	Select which TRE and DW bits are sent to the HRDREQ read request pins. HRDREQ = (DMA_DW and OSEL_0) or (VCX_DW and OSEL_1) or (DBG_DW and OSEL_2).
3:1	ISEL[2:0]	Select which TRE and DW bits are sent to the HWRREQ (write request) pins. HWRREQ = (DMA_TRE and ISEL_0) or (VCX_TRE and ISEL_1) or (DBG_TRE and ISEL_2).
0	CLR_ RIRQ	RISC-to-Host IRQ Clear. Writing a 1 to this bit clears the RISC to host IRQ.

H_HOSTMASK (0x4, R/W)

ENDN_ SEL	DBG_ TRE	DBG_DW	DMA_ TRE	DMA_DW	VCXI _TRE	VCXI _DW	R2R_IRQ
7	6	5	4	3	2	1	0

The Host Interface IRQ Mask register After reset, it is initialized to 0x00.

Bits	Name	Description
7	ENDN_ SEL	Host Side Endian Select. When set, this bit switches the upper and lower bytes of data sent as writes to the Host Interface DMA Port register. 1 = switch upper/lower bytes.
6	DBG_ TRE	Debug Transmit Register Empty Enable.
5	DBG DW	Debug data waiting 1 = Host ready to read debug data from ESS RISC.
4	DMA TRE	DMA transmit register empty. 1 = Host ready to send DMA data to ESS RISC.
3	DMA DW	DMA data waiting 1 = Host waiting to read data from ESS RISC.
2	VCXI TRE	VCXI transmit register empty 1 =Host ready to send data to ESS RISC.
1	VCXI DW	VCXI data waiting 1 = Host waiting to read data from ESS RISC.
0	R2R IRQ	Interrupt flag 1 = Set by ESS RISC as Ready To Receive signal to the host.

H_HOSTIRQSTAT (0x5, R)

H2RIRQ	DBGTRE	DBGDW	DMATRE	DMADW	VCXITRE	VCXIDW	R2HIRQ
7	6	5	4	3	2	1	0

This register reads the status of Interrupts from the RISC to the host; 1=IRQ, 0=no IRQ.

Bits	Name	Description
7	H2R IRQ	Interrupt flag set by the host as a signal to the RISC.
6	DBG TRE	Debug transmit register empty (OK for host to send data to the RISC).
5	DBG DW	Debug data waiting (host needs to read data from the RISC).
4	DMA TRE	DMA transmit register empty (OK for host to send data to the RISC).
3	DMA DW	DMA data waiting (host needs to read data from the RISC).
2	VCXI TRE	VCXI transmit register empty (OK for host to send data to the RISC).
1	VCXI DW	VCXI data waiting (host needs to read data from the RISC).
0	R2H IRQ	Interrupt flag set by the RISC as a signal to the host.

Video Interface Registers

The following describes the video interface registers.

Video Output Registers

VID_SCN_HSTART (0x20001000h, W)

—	HSTART
15:13	12:0

The Video Screen Horizontal Start register contains the 13-bit horizontal pixel starting address of the active window for the screen.

Bits	Name	Description
15:13	–	Reserved.
12:0	HSTART	Horizontal start of active window.

VID_SCN_HEND (0x20001004h, W)

—	HEND
15:13	12:0

The Video Screen Horizontal End register contains the 13-bit horizontal pixel end address of the active window for the screen.

Bits	Name	Description
15:13	–	Reserved.
12:0	HEND	Horizontal end of active window.

VID_SCN_VSTART (0x20001008h, W)

—	VSTART
15:13	12:0

The Video Screen Vertical Start register contains the 13-bit vertical scan line starting address of the active window for the screen.

Bits	Name	Description
15:13	–	Reserved.
12:0	VSTART	Vertical start of active window.

VID_SCN_VEND (0x2000100Ch, W)

—	VEND
15:13	12:0

The Video Screen Vertical End register contains the 13-bit vertical scan line ending address of the active window for the screen.

Bits	Name	Description
15:13	–	Reserved.
12:0	VEND	Vertical end of active window.

VID_SCN_VERTIRQ (0x20001010h, W)

—	VERTIRQ
15:13	12:0

The Video Screen Vertical Line Interrupt write-only register is selectable by software and contains the line in which a vertical interrupt will occur. Line 0 is the top of the screen (leading edge of VSYNC pin). Typical is to set an interrupt either just before or just after the active region of the screen.

Bits	Name	Description
15:13	–	Reserved.
12:0	VERT IRQ	Line where a vertical interrupt will occur.

VID_SCN_HBLANK_START (0x20001014h, W)

—	HBLANK_START
15:13	12:0

The Video Screen Horizontal Blanking Start write-only register contains the 13-bit starting address of the horizontal blanking interval.

Bits	Name	Description
15:13	–	Reserved.
12:0	HBLANK_ START	Start of horizontal blanking interval.

VID_SCN_HBLANK_STOP (0x20001018h, W)

—	HBLANK_STOP
15:13	12:0

This register contains the ending address of the horizontal blanking.

Bits	Name	Description
15:13	–	Reserved.
12:0	HBLANK STOP	End of horizontal blanking.

VID_SCN_VBLANK_START (0x2000101Ch, W)

—	VBLANK_START
15:13	12:0

The Video Screen Vertical Blanking Start register contains the starting address of the vertical blanking interval.

Bits	Name	Description
15:13	–	Reserved.
12:0	VBLANK START	Start of vertical blanking interval.

VID_SCN_VBLANK_STOP (0x20001020h, W)

—	VBLANKSTOP
15:13	12:0

This register contains the ending address of the vertical blanking.

Bits	Name	Description
15:13	–	Reserved.
12:0	VBLANK STOP	End of vertical blanking.

VID_SCN_HSYNCWIDTH (0x20001024h, W)

—	HSYNCWIDTH
15:13	12:0

This register contains the width of the horizontal sync pulse. It is needed only if sync direction is output.

Bits	Name	Description
15:13	–	Reserved.
12:0	HSYNC WIDTH	Horizontal sync pulse width.

VID_SCN_HSYNCPERIOD (0x20001028h, W)

—	HSYNCPERIOD
15:13	12:0

This register contains the period of the horizontal sync pulse. It is needed only if sync direction is output.

Bits	Name	Description
15:13	–	Reserved.
12:0	HSYNC PERIOD	Horizontal sync period.

VID_SCN_VSYNCPERIOD (0x2000102Ch, W)

—	VSYNCPERIOD
15:13	12:0

This register contains the period of the vertical sync pulse. It is needed only if sync direction is output.

Bits	Name	Description
15:13	–	Reserved.
12:0	VSYNC PERIOD	Vertical sync pulse period.

VID_SCN_VSYNCPIXEL (0x20001030h, W)

—	VSYNCPIXEL
15:13	12:0

This register defines which pixel VSYNC will change on. The number of pixels delayed from HSYNC that VSYNC will change on (rise or fall). This is needed only if sync direction is output.

Bits	Name	Description
15:13	–	Reserved.
12:0	VSYNC PIXEL	Pixel on which VSYNC will change.

VID_SCN_VSYNCWIDTH (0x20001034h, W)

—	VSYNCWIDTH
15:6	5:0

This register defines the width of the vertical sync pulse. It is needed only if sync direction is output.

Bits	Name	Description
15:6	–	Reserved.
5:0	VSYNC WIDTH	Vertical sync pulse width.

VID_SCN_VERTCOUNT (0x20001036h, R)

—	VERTCOUNT
15:13	12:0

For testing only. This register contains the current line of the vertical counter. Starts at VSYNC line 0.

Bits	Name	Description
15:13	–	Reserved.
12:0	VERT COUNT	Current pixel of the vertical counter.

VID_SCN_HORIZCOUNT (0x20001038h, R)

—	HORIZCOUNT
15:13	12:0

For testing only. This register contains the current pixel of the horizontal counter. Starts at HSYNC pixel 0.

Bits	Name	Description
15:13	–	Reserved.
12:0	HORIZ COUNT	Current pixel of the horizontal counter.

VID_SCN_COUNTER_CTL (0x2000103Ch, W)

—	INVBLNK	0	INVHS	INVVS	MSTR MODE
7:5	4	3	2	1	0

This register contains miscellaneous counter control bits. After reset, it is initialized to 0x00.

Bits	Name	Description
7:5	–	Reserved.
4	INV BLNK	Inverted blank sync. 1 = blank is active low. 0 = otherwise.
3	–	Set at zero.
2	INVHS	Inverted horizontal sync. 1 = horizontal sync is active low.
1	INVVS	Inverted vertical sync. 1 = vertical sync is active low. 0 = otherwise.
0	MSTR MODE	Master Mode Select. 1= Vibratto drives sync pins. 0= Syncs input to Vibratto.

VID_SCN_OUTPUTCNTL (0x20001040h, R/W)

—	ZEROB	BYPASS	3TAP _EN	COEF LDMD	CLAMP _EN	INV MSB	YUV 8BIT	TS MODE
15:9	8	7	6	5	4	3:2	1	0

This register contains the mode bits used to control video output.

Bits	Name	Description
15:9	—	Reserved.
8	ZEROB	Zero Boundary. 1 = Use zeroes for pixels outside of the border for horizontal filtering. 0 = Use the pixel on the edge.
7	BYPASS	Horizontal Filter Bypass. 1 = Bypass horizontal filter. 0 = Use horizontal filter.
6	3TAP_EN	3/7 Tap Filter Select. 1 = 3-tap horizontal filter selected. 0 = 7-tap horizontal filter selected.
5	COEF LDMD	0 = UV is selected first. 1 = Y is selected first.
4	CLAMP _EN	Clamp Enable. 1 = Clamp output according to CCIR601 min/max values. 0 = No clamping.
3:2	INVMSB [1:0]	Invert MSB YUV Output [1:0]. INVMSB[1] = Invert MSB of Y output. INVMSB[0] = Invert MSB of UV output.
1	YUV8BIT	8-bit YUV Output Enable. 1 = 8-bit YUV output enabled 0 = Invalid.
0	TSMODE	Toggle Select Mode. 1 = Y is first in 8-bit mode. 0 = UV is first in 8-bit mode.

VID_SCN_ITERFACECNTL (0x20001048h, R/W)

—	MM	MBM	INVHS	INVVS	INVB	1PE	EPU	MCK	CLKDIV	IPQ	CK1M
15:12	11	10	9	8	7	6	5	4	3:2	1	0

This register contains the mode bits used to control video output.

Bits	Name	Description
15:12	—	Reserved.
11	MM	Master Mode. 1 = Vibratto drives sync signals. 0 = Slave mode.
10	MBM	Master Blanking Mode 1 = Vibratto determines blanking region. 0 = Slave mode.
9	INVHS	Invert Horizontal Sync. 1 = Horizontal sync inverted.
8	INVVS	Invert Vertical Sync. 1 = Vertical sync inverted.
7	INVB	Invert Blanking. 1 = Blanking interval inverted.
6	1PE	First Pixel Even. 1 = First pixel of active region is even.
5	EPU	Even Pixel U Select. 1 = Even pixel is U pixel. 0 = Even pixel is V pixel.
4	MCK	Master Pixel Clock Mode. 1 = Vibratto drives master clock.
3:2	CLK_DIV [1:0]	Clock Divider [1:0]. Vibratto drives pixel clocks: I

CLK DIV1	CLK DIV0	Description
0	0	Screen clock depends on CLK1XMOD (default).
0	1	13.5 MHz screen clock is half of input pixel clock.
1	X	6.75 MHz screen clock is one-quarter of input pixel clock.

Bits	Name	Description
1	IPQ	Invert PCLKQSCN. 1 = PCLKQSCN pin inverted.
0	CK1M	Clock1X Mode. 1 = Use PCLK2XSCN or internal 27 MHz PCLK 0 = Use 13.5 MHz PCLKQSCN.

VID_SCN_RESETS (0x20001050h, R/W)

—	R_PAN	1	R_Y	R_UV	R_HF	R_CNT	DMAGO
15:8	7	6:5	4	3	2	1	0

Resets for the video screen section. These bits are set to 1 on reset.

Bits	Name	Description
15:8	–	Reserved.
7	R_PAN	Reset Pan and Scan. 1 = Reset pan and scan function (default).
6:5	1	Reserved. Always 1.
4	R_Y	Reset Y FIFO. 1 = Reset Y FIFO (default).
3	R_UV	Reset UV FIFO. 1 = Reset UV FIFO (default).
2	R_HF	Reset Horizontal Filter. 1 = Horizontal filter reset (default).
1	R_CNT	Reset Counter. 1 = Counter reset (default)
0	DMAGO	DMA Enable. 1 = DMA enabled (default).

VID_SCN_STATUS (0x20001058h, R)

O_E	BLNK	HS	VS	VACT	ACT	ACT D1	ACT D2	ACT D3	1P	NL	NF	NP	EP	UP	UP D!
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

This register contains the status bits for the video section.

Bits	Name	Description
15	O_E	VS/HS Odd or Even Field Status. 1 = Odd field. 0 = Even field.
14	BLNK	status of internal blanking.
13	HS	Status of internal horizontal sync.
12	VS	Status of internal vertical sync.
11	VACT	Vertical Active.
10	ACT	Active Screen for FIFO.
9	ACT_D1	Active Horizontal Filter Signal. 1 = Horizontal filtering signal active.
8	ACT_D2	Active OSD/SPU/Mixer Signal. 1 = OSD/SPU/Mixer signal active.
7	ACT_D3	Active Output Port Signal. 1 = Output port signal active.
6	1P	First Active Pixel for FIFO. 1 = First active pixel selected.
5	NL	New Line. 1 = First pixel of new line selected.
4	NF	New Field. 1 = First pixel of new field selected.
3	NP	New Pixel. 1 = One clock cycle of every pixel clock cycle selected.
2	EP	Even Pixel for FIFO. 1 = Current pixel selected for FIFO is even.
1	UP	U Pixel Horizontal Filter Select. 1 = Current pixel uses U for horizontal filtering. 0 = Current pixel uses V for horizontal filtering.
0	UPD1	U Pixel Mixer Select. 1 = Current pixel uses U for OSD/SPU/Mixer. 0 = Current pixel uses V for OSD/SPU/Mixer.

On Screen Display (OSD) Controller Registers

VID_SCN_OSD_HSTART (0x20001110h, R/W)

—	OSD_HSTART
15:13	12:0

This register contains the horizontal starting address (referenced from active window).

Bits	Name	Description
15:13	–	Reserved.
12:0	OSD_ HSTART	Horizontal starting address.

VID_SCN_OSD_HEND (0x20001114h, R/W)

—	OSD_HEND
15:13	12:0

This register contains the horizontal ending address (referenced from active window).

Bits	Name	Description
15:13	–	Reserved.
12:0	OSD_ HEND	Horizontal ending address.

VID_SCN_OSD_VSTART (0x20001118h, R/W)

—	OSD_VSTART
15:13	12:0

This register contains the vertical starting address (referenced from active window).

Bits	Name	Description
15:13	–	Reserved.
12:0	OSD VSTART	Vertical starting address.

VID_SCN_OSD_VEND (0x2000111Ch, R/W)

—	OSD_VEND
15:13	12:0

This register contains the OSD vertical ending address (referenced from active window).

Bits	Name	Description
15:13	–	Reserved.
12:0	OSD_ VEND	Vertical ending address.

VID_SCN_OSD_MISC (0x20001124h, R/W)

LAT_INT	RESET_OVERLAY	PAL_INDEX [1:0]	INTEN	LDMD	MODE
7	6	5:4	3	2	1:0

This register contains miscellaneous control and status bits in the OSD controller.

Bits	Name	Description
7	LAT_INT	Latched interrupt. This is a read-only bit.
6	RESET_ OVERLAY	Reset overlay section (set to 1 at reset).
5:4	PAL_ INDEX	Upper 2 bits of palette address when in 2-bit mode.
3	INTEN	Interrupt enable.
2	LDMD	Enable palette load.

Bits	Name	Description
1:0	MODE	0 0 = Bypass (initializes to 00 at reset). 0 1 = 2 bit/pixel. 1 0 = 4 bit/pixel. 1 1 = 8 bit/pixel.

VID_SCN_ OSD_PALETTE (0x20001140h–0x2000117Ch, R/W)

Y	V
15:12	11:8

U	BLND_ON/OFF	BLND
7:4	3	2:0

These 16 registers contain the OSD palette.

Bits	Name	Description
15:12	Y	Upper 4 bits of luminance data (lower 4 bits are 0).
11:8	V	Upper 4 bits of V chrominance data (lower 4 bits are 0).
7:4	U[	Upper 4 bits of U chrominance data (lower 4 bits are 0).
3	BLND_ ON/OFF	Blending/Transparency Enable. 1 = Blending off; transparency on. 0 = Blending on; transparency off.
2:0	BLND	Blending value: value blnd value blnd 0 1/8 4 5/8 1 2/8 5 6/8 2 3/8 6 7/8 3 4/8 7 8/8 finalpixel = blnd x palette value + (1 - blnd) x original pixel.

For mode 3 (8-bit/pixel) the upper 4 bits of the pixel are the blend information, the lower 4 bits are the palette index and the blend information in the palette is ignored.

Subpicture Unit (SPU) Decoder Registers

This section describes the Subpicture Unit (SPU) decoder registers.

SP_SPCTL (0x20001600h, R/W)

—	RESET2	SP_REL
15:10	9	8

CCIRQ EN	RISC_ DONE	SPUON	RESET	RLEAT	DCSEAT	RLIRQEN	DCSIRQ EN
7	6	5	4	3	2	1	0

This register is the Sub-Picture Control register. After reset, it is initialized to 0x000h. Write a “1” to the corresponding bit to mask the interrupt.

Bits	Name	Description
15:10	—	Reserved.
9	RESET2	Write only: 1 = Reset part of SPU (i.e., similar to reset at the end of a frame); the FIFOs and the state machines are reset, but not the registers (one clock cycle). 0 = Nothing. Need to kill DMA and set this bit before every frame if DMA is not exact.
8	SP_REL	0 = Coordinates for changes within the Sub-Picture are relative to the main video display area. 1 = Coordinates for changes within the Sub-Picture are relative to the Sub-Picture.
7	CCIRQ_ EN	1 = Col/con command error interrupt enable. 0 = Disabled.
6	RISC_ DONE	Write only: 1 = RISC done with decoding SP (one clock cycle). 0 = Otherwise.
5	SPUON	Sub-Picture on/off: 1 = Sub-Picture is on. 0 = Sub-Picture is off.
4	RESET	Write only: 1 = Reset SPU decoder (one clock cycle). 0 = Otherwise.
3	RLEAT	RISC eat RLFIFO: 0 = RISC read FIFO output only, no change in value. 1 = RISC read FIFO, causes it to eat byte.
2	DCSEAT	RISC eat DCSFIFO: 0 = RISC read FIFO output only, no change in value. 1 = RISC read FIFO, causes it to eat byte.
1	RLIRQ EN	1 = RLFIFO IRQ enable. 0 = RLFIFO IRQ disable.
0	DCSIRQ EN	1 = DCSFIFO IRQ enable. 0 = DCSFIFO IRQ disable.

SP_VCNT (0x20001700h, R/W)

—	SP_VCNT
15:10	9:0

This register is the Vertical Counter Value register. After reset, it is initialized to 0x07Fh.

Bits	Name	Description
15:10	—	Reserved.
9:0	SP_VCNT	SPU vertical count value.

SP_VCNTREG (0x20001704h, R/W)

—	SP_VCNT_INIT
15:10	9:0

This register is the Vertical Counter Initial Value register. After reset, it is initialized to 0x7FEh

Bits	Name	Description
15:11	—	Reserved.
10:0	SP_VCNT INIT	SPU vertical count initial value.

SP_HCNT (0x20001708h, R/W)

—	SP_HCNT
15:11	10:0

This register is the Horizontal Counter Value register. After reset, it is initialized to 0x0h.

Bits	Name	Description
15:11	—	Reserved.
10:0	SP_HCNT	SPU horizontal count value.

SP_HCNTREG (0x2000170Ch, R/W)

—	SP_HCNT_INIT
15:10	9:0

This register is the Horizontal Counter Initial Value register. After reset, it is initialized to 0x000h.

Bits	Name	Description
15:10	—	Reserved.
9:0	SP_HCNT INIT	SPU horizontal count initial value.

SP_VSTART (0x20001710h, R/W)

—	SP_VSTART
15:10	9:0

SP_VSTART is the Start Line of Subpicture display area register. After reset, it is initialized to 0x3FFh.

Bits	Name	Description
15:10	—	Reserved.
9:0	SP_VSTART	SPU vertical start line value.

SP_VEND (0x20001714h, R/W)

—	SP_VEND
15:10	9:0

SP_VEND is the End Line of Subpicture display area register. After reset, it is initialized to 0x3FFh.

Bits	Name	Description
15:10	—	Reserved.
9:0	SP_VEND	SPU vertical start line value.

SP_HSTART (0x20001718h, R/W)

—	SP_HSTART]
15:10	9:0

SP_HSTART is the Horizontal Start Pixel of the Subpicture display area register. After reset, the contents of this register is initialized to 0x3FFh.

Bits	Name	Description
15:10	—	Reserved.
9:0	SP_HSTART	SPU horizontal start pixel value.

SP_HEND (0x2000171Ch, R/W)

—	SP_HEND
15:10	9:0

SP_HEND is the Horizontal Pixel End of the Subpicture display area register. After reset, it is initialized to 0x3FFh.

Bits	Name	Description
15:10	—	Reserved.
9:0	SP_ HEND	SPU horizontal end pixel value.

SP_SUBVCNT (0x20001720h, R/W)

—	SP_SUBVCNT
15:10	9:0

SP_SUBVCNT is the Subpicture Vertical Count register within the Subpicture display area register. After reset, it is initialized to 0x3FFh.

Bits	Name	Description
15:10	—	Reserved.
9:0	SP_SUB VCNT	SPU subpicture display vertical count value.

SP_SUBHCNT (0x20001724h, R/W)

—	SP_SUBHCNT
15:10	9:0

SP_SUBHCNT is the Horizontal Pixel Count within the Subpicture display area register. After reset, it is initialized to 0x3FFh.

Bits	Name	Description
15:10	—	Reserved.
9:0	SP_SUBHCNT	SPU subpicture display horizontal pixel count value.

SP_VCSTART (0x20001728h, R/W)

—	SP_VCSTART
15:10	9:0

SP_VCSTART is the Start Line of Current Sub-Picture Change register. After reset, it is initialized to 0x3FFh.

Bits	Name	Description
15:10	—	Reserved.
9:0	SP_VCSTART	SPU current subpicture display vertical start scan line value.

SP_VCEND (0x2000172Ch, R/W)

—	SP_VCEND
15:10	9:0

SP_VCEND is the End Line of Current Subpicture Change register. After reset, it is initialized to 0x3FFh.

Bits	Name	Description
15:10	—	Reserved.
9:0	SP_VCEND	SPU current subpicture display vertical end scan line value.

SP_HIVS (0x20001730h, R/W)

—	SPU_HIVS
15:10	9:0

SP_HIVS is the current subpicture Highlight Vertical Start Line display area register. After reset, it is initialized to 0x3FFh.

Bits	Name	Description
15:10	—	Reserved.
9:0	SPU_HIVS	SPU current subpicture display highlight vertical start scan line value.

SP_HIVE (0x20001734h, R/W)

—	SPU_HIVE
15:10	9:0

SP_HIVE is the current subpicture Highlight Vertical End Line display area register. After reset, it is initialized to 0x3FFh.

Bits	Name	Description
15:10	—	Reserved.
9:0	SPU_HIVE	SPU current subpicture display highlight vertical end scan line value.

SP_HIHS (0x20001738h, R/W)

—	SPU_HIHS
15:10	9:0

SP_HIHS is the current subpicture Highlight Horizontal Start Pixel display area register. After reset, it is initialized to 0x3FFh.

Bits	Name	Description
15:10	—	Reserved.
9:0	SPU_HIHS	SPU current subpicture display highlight horizontal pixel start value.

SP_HIHE (0x2000173Ch, R/W)

—	SPU_HIHE
15:10	9:0

SP_HIHE is the current subpicture Highlight Horizontal End Pixel display area register. After reset, it is initialized to 0x3FFh.

Bits	Name	Description
15:10	—	Reserved.
9:0	SPU_HIHE	SPU current subpicture display highlight horizontal pixel end value.

SP_HSTART1-8 (0x20001740h–0x200175Ch, R/W)

—	SPU_HSTART
15:10	9:0

SP_HSTART [1:8] are the Pixel Number for Start of Changes 1 Through 8 register. After reset, the contents of these registers are initialized to 0x3FF.The register bit tables for all these registers are identical to the one shown above.

Bits	Name	Description
15:10	—	Reserved.
9:0	SPU_HSTART	SPU current subpicture display highlight horizontal pixel change start value.

SP_VTCTL (0x20001760h, R/W)

NUMCHG	CINDEX	CS	CC PAR SEEN	RLEN	CHG VAL ID	HI VAL ID
15:12	11:8	7:4	3	2	1	0

This register is the Subpicture Display Video Timing Control register. After reset, it is initialized to 0x0000.

Bits	Name	Description
15:12	NUMCHG	Number of changes in current horizontal stripe.
11:8	CINDEX	Code index (current region index).
7:4	CS	Current state of COL/CON state machine (read only).
3	CCPA_ SEEN	1 = Start parsing COL/CON data (one clock cycle) (need to set after RISC decodes). 0 = Otherwise.
2	RLEN	1 = Current pixel in subpicture display area. 0 = Otherwise.
1	CHG VAL ID	1 = Current pixel is within a change region (i.e., not default subpicture color/contrast). 0 = Otherwise.
0	HI VAL ID	1 = Current pixel is within the highlight region. 0 = Otherwise.

SPU Contrast Index Registers

This section describes the Contrast Index registers in the SPU decoder.

SP_CON0 (0x200017B0h, R/W)

D	C	B	A
15:12	11:8	7:4	3:0

SP_CON0 through SP_CON9 are registers containing the contrast index for a particular region and pixel type. SP_CON0 is the default Subpicture Display Start Contrast region register. After reset, it is initialized to 0x0000h.The register bit tables for all these registers are identical to the one shown above.

Bits	Name	Description
15:12	D	Contrast index for emphasis 2 pixel (type 11).
11:0	C	Contrast index for emphasis 1 pixel (type 10).
7:4	B	Contrast index for pattern pixel (type 01).
3:0	A	Contrast index for background pixel (type 00).

SP_CON1:8 (0x200017B4h–0x200017D0h, R/W

D	C	B	A
15:12	11:8	7:4	3:0

SP_CON0 through SP_CON9 are registers containing the contrast index for a particular region and pixel type. SP_CON1 through SP_CON8 are the change region registers. After reset, each register is initialized to 0x0000h. The register bit tables for all of these registers are identical to the one shown above.

Bits	Name	Description
15:12	D	Contrast index for emphasis 2 pixel (type 11).
11:0	C	Contrast index for emphasis 1 pixel (type 10).
7:4	B	Contrast index for pattern pixel (type 01).
3:0	A	Contrast index for background pixel (type 00).

SP_CON9 (0x200017D4h, R/W)

D	C	B	A
15:12	11:8	7:4	3:0

SP_CON0 through SP_CON9 are registers containing the contrast index for a particular region and pixel type. SP_CON9 is the highlight region register. After reset, it is initialized to 0x0000h. The register bit tables for all these registers are identical to the one shown above.

Bits	Name	Description
15:12	D	Contrast index for emphasis 2 pixel (type 11).
11:0	C	Contrast index for emphasis 1 pixel (type 10).
7:4	B	Contrast index for pattern pixel (type 01).
3:0	A	Contrast index for background pixel (type 00).

SPU Color Index Registers

This section describes the Color Index registers in the SPU decoder.

SP_COL0 (0x20001780h, R/W)

D	C	B	A
15:12	11:8	7:4	3:0

SP_COL0 through SP_COL9 are registers containing color index for a particular region and pixel type. COL0 is the default Subpicture Display Start Color region register. After reset, it is initialized to 0x0000h. The register bit tables for all these registers are identical to the one shown above.

Bits	Name	Description
15:12	D	Color index for emphasis 2 pixel (type 11).
11:0	C	Color index for emphasis 1 pixel (type 10).
7:4	B	Color index for pattern pixel (type 01).
3:0	A	Color index for background pixel (type 00).

SP_COL1:8 (0x20001784h–0x20017A0h, R/W)

D	C	B	A
15:12	11:8	7:4	3:0

SP_COL0 through SP_COL9 are registers containing color index for a particular region and pixel type. SP_COL1:8 are the change region 1-8 registers. After reset, each register is initialized to 0x0000.

NOTE : The register bit tables for all of these registers are identical to the one shown above.

Bits	Name	Description
15:12	D	Contrast index for emphasis 2 pixel (type 11).
11:0	C	Contrast index for emphasis 1 pixel (type 10).
7:4	B	Contrast index for pattern pixel (type 01).
3:0	A	Contrast index for background pixel (type 00).

SP_COL9 (0x200017A4h, R/W)

D	C	B	A
15:12	11:8	7:4	3:0

SP_COL0 through SP_COL9 are registers containing color index for a particular region and pixel type. SP_COL9 is the highlight region register. After reset, it is initialized to 0x0000.

NOTE : The register bit tables for all these registers are identical to the one shown above.

Bits	Name	Description
15:12	D[3:0]	Color index for emphasis 2 pixel (type 11).
11:0	C[3:0]	Color index for emphasis 1 pixel (type 10).
7:4	B[3:0]	Color index for pattern pixel (type 01).
3:0	A[3:0]	Color index for background pixel (type 00).

Host Interface (RISC Side) Registers

The following describes the host interface RISC side registers.

R_HOSTDMAPORT (0x20003000h, R/W)

(RISC side) Host Interface DMA Port
15:0

This register contains data transferred to/from the host (DMA port). After reset, it is initialized to 0x0000.

R_HOSTVCXPORT (0x20003004h, R/W)

(RISC side) Host Interface Command Port
7:0

This register contains data transferred to/from the host (VCX port). After reset, it is initialized to 0x00.

R_HOSTDBGPORT (0x20003008h, R/W)

(RISC side) Host Interface Debug Port
7:0

This register contains data transferred to/from the host (debug port). After reset, it is initialized to 0x00.

R_HOSTMASK (0x20003010h, R/W)

ENDNSEL	DBGDW	DBGTRE	DMADW	DMATRE	VCXIDW	VCXITRE	H2RIRQ
7	6	5	4	3	2	1	0

This register contains the mask bits for interrupts from the host to the RISC. After reset, it is initialized to 0x0.

Bits	Name	Description
7	ENDN_SEL	Big/Little Endian Select 1 = switch upper/lower bytes when write R_HOSTDMAPORT.
6:0		Mask bits for interrupts from the host to the RISC.

R_HOSTIRQSTAT (0x20003014h, R)

—	DCI ERR	DCI IRQ	R2H IRQ	DBG TRE	DBG DW	DMA TRE	DMA DW	VCXI TRE	VCXI DW	H2R IRQ
15:10	9	8	7	6	5	4	3	2	1	0

This register reads the status of interrupts from the host to the RISC; 1=IRQ, 0=no IRQ.

Bits	Name	Description
15:10	—	Reserved.
9	DCIERR	DCI Sector Error Detect. 1 = previous sector has error.
8	DCIIRQ	Sector-end interrupt from DCI port to RISC.
7	R2HIRQ	Interrupt flag set by the RISC as a signal to the host.
6	DBG TRE	Debug transmit register empty (OK for RISC to send data to the host).
5	DBGDW	Debug data waiting (RISC needs to read data from the host).
4	DMA TRE	DMA transmit register empty (OK for RISC to send data to the host).
3	DMA DW	DMA data waiting (RISC needs to read data from the host).
2	VCXI TRE	VCXI transmit register empty (OK for RISC to send data to the host).
1	VCXI DW	VCXI data waiting (RISC needs to read data from the host).
0	H2RIRQ	Interrupt flag set by the host as a signal to the RISC.

R_IDEDAT (0x20003018h, R/W)

IDE_DATA
15:0

This register contains data sent/received to/from ATAPI slave, in master mode. After reset, it is initialized to 0x0000h.

R_IDEADDR (0x2000301Ch, R/W)

—	IDE_ADDR
7:3	2:0

This register contains address sent to ATAPI slave, in master mode. After reset, it is initialized to 0x0.

R_IDECTL (0x20003020h, R/W)

—	CLRIRQ	IDE2XPT	IDEST	IDERST	IDEMSK1
15:13	12	11	10	9	8

IDEMSK0	IDECS	HSTMODE	IDE_EN	IDE_RW	PIO MODE
7	6	5	4	3	2:0

After reset, it is initialized to 0x0000h.

Bits	Name	Description
15:13	–	Reserved.
12	CLRIRQ	Write 1 to clear sector-end interrupt from ATAPI slave.
11	IDE2 XPT	In master mode, write 1 to this bit to enable data transfer from ATAPI data port to RISC. Data transfer will continue on until this bit is reset to 0.
10	IDEST	write 1 to signal the beginning of the sector. The sector start signal will be reset by the first data valid.
9	IDERST	Write 1 to reset the ATAPI slave, then write 0 to unreset. The ATAPI slave will also be reset at the same time with the ES4427.
8	IDE MSK1	Mask sector-end interrupt from ATAPI to RISC.
7	IDE MSK0	Mask interrupt from ATAPI to RISC.
6	IDECS	IDE Chip Select 1 = Assert cs3fxb. 0 = Assert cs1fxb.
5	HST MODE	0 = slave mode. Host will receive commands or data from DVD-DSP. 1 = master mode. Host will send read/write commands (comply to ATAPI).
4	IDEEN	Enable the host to write/read to/from the ATAPI slave.
3	IDERW	1 = Read from ATAPI slave. 0 = Write to ATAPI slave.
2:0	PIO MODE [2:0]	PIO Mode Select [2:0].

R_IDESSTAT (0x20003024h, W)

—	IDEIRQ	IDE16	IDEVAL
7:3	2	1	0

Bits	Name	Description
7:3	-	Reserved.
2	IDEIRQ	1 = Sector-end interrupt from ATAPI slave to RISC.
1	IDE16	Read only bit 1 = 16-bit transfer. If reading from ATAPI slave, all 16-bit data of R_IDEDAT are valid. If writing to ATAPI slave, all 16-bit data of R_IDEDAT are received at the ATAPI slave. 0 = 8-bit transfer. If reading from ATAPI slave, only the last 8 bits of R_IDEDAT are valid. If writing to ATAPI slave, only the last 8 bits of R_IDEDAT are received at the ATAPI slave.
0	IDEVAL	1 = PIO cycle is completed. In read mode, read from R_IDEDAT to retrieve the data from the ATAPI slave; write 1 to clear this bit.

R_IDECNT (0x20003028h, R/W)

—	IDE CNT
15:12	11:0

After reset, it is initialized to 0x07FFh.

Bits	Name	Description
15:12		Reserved.
11:0	IDECNT	In master/dci mode, program this register to the sector size. In master mode, reading from this register will reveal the count down value.

R_DCICTL **(0x2000302Ch, R/W)**

—	IORMSK	ACKLVL	REQLVL	SYNCNUM	SYNCLVL	DELAY	LDR_SEL
31:12	11	10	9	8	7	6:2	1:0

This register controls the host port when the Vibratto is in DCI mode. After reset, it is initialized to 0x000h.

Bits	Name	Description
31:12		Reserved.
11	IORMSK	I/O Ready Mask Enable. 1 =Mask I/O ready (default). 0 = Don't mask.
10	ACKLVL	Acknowledge Level. 1 = ACK level active-high. 0 = ACK level active-low.
9	REQLVL	Request Level. 1 = Original and delayed sector starts. 0 = Original sector start.
8	SYNC NUM	Sync Number. 1 = Original and delayed sector starts. 0 = Original sector start
7	SYNC LVL	Sync Level. 1 = SYNC level active-high. 0 = SYNC level active-low.
6:2	DEL[4:0]	Delay Sector Start Cycles.
1:0	LDRSEL	Loader Select [1:0]

LDR SEL1	LDR SEL0	Description
0	0	Bypass mode.
0	1	Sanyo loader
1	0	Takaya loader.
1	1	SGS-Thomson loader.

Host Interface (RISC-SRAM Interface) Registers

The section describes the RISC-SRAM interface registers.

RIFACE_WIDTH **(0x20004000h, R/W)**

—	DBGMODE	CACHEFLS	CACHE DISABLE	DIV2:0	B3W	B2W	B1W	B0W
15:11	10	9	8	7:5	4	3	2	1:0

This register contains the width of the bus to external memory, and controls the internal cache. The value of the TDMDX pin is sampled at the rising edge of RESET# and the RIFACE_WIDTH register is programmed according to the bit settings of the following table.

TDMDX/RSEL	Selection
0	8-bit ROM.
1	16-bit ROM.

Bits	Name	Description
15:11	–	Reserved.
10	DBGMODE	Debug mode: 0 = Save power from outside pins toggling. 1 = riscaddr and riscbus are seen from the SRAM address/data. Resets to 1.
9	CACHE_FLS	Cache flush: 1 = flush. Resets to 1.
8	CACHE DISABLE	Cache disable signal: 0 = Cache enabled. 1 = Cache bypassed. Resets to 1 (Cache disabled).
7:5	DIV[2:0]	Clock Divisor.
4	B3W	Bank 3 Width 1 = 16 bits wide. 0 = 8 bits wide (default).
3	B2W	Bank 2 Width 1 = 16 bits wide. 0 = 8 bits wide (default).
2	B1W	Bank 1 Width 1 = 16 bits wide. 0 = 8 bits wide (default).
1:0	B0W	Bank 0 Width [1:0] 00 = 8-bit wide (default). 01 = 16-bit wide. 10 = Map Bank 0 to DRAM. 11 = Undefined.

.RIFACE_WAIT_STATE (0x20004004h, R/W)

—	BANK3	BANK2	BANK1	BANK0
31:20	19:15	14:10	9:5	4:0

This register contains the number of external wait states (from 1 to 32) per access for banks 0-3. The table below gives the hexadecimal value for the number of wait states:

Hex Value	Wait State	Hex Value	Wait State	Hex Value	Wait State	Hex Value	Wait State
1F	1	17	9	0F	17	07	25
1E	2	16	10	0E	18	06	26
1D	3	15	11	0D	19	05	27
1C	4	14	12	0C	20	04	28
1B	5	13	13	0B	21	03	29
1A	6	12	14	0A	22	02	30
19	7	11	15	09	23	01	31
18	8	10	16	08	24	00	32 (default)

RIFACE_AUX1 (0x2000402Ch, R/W)

—	0	T3	T2	P3	P2	P1	P0
15:10	9:6	5	4	3	2	1	0

This register is a general I/O port for interfacing with external devices.

Bits	Name	Description
15:10	–	Reserved.
9:6	—	Reserved. Always 0.
5:4	T3,T2	Tri-state controls. 1 = I/O state selected. 0 = Tri-state selected.
3	P3	Tri-stateable pin.
2	P2	Tri-stateable pin.
1	P1	Open collector pin.
0	P0	Open collector pin.

When this register is read, the values read are the values at the pin. The two open collector pins allow I^2C bus communication and require an external pull-up resistor. The default value is for P3:P2 to be tri-state, and P1:P0 to be disabled (i.e., P1, P0 = high (logic 1), and T3, T2 = low (logic 0)).

RIFACE_AUX2 (0x20004030h, R/W)

—	AUX7_IS_STALL	T	P
15:9	8	7:4	3:0

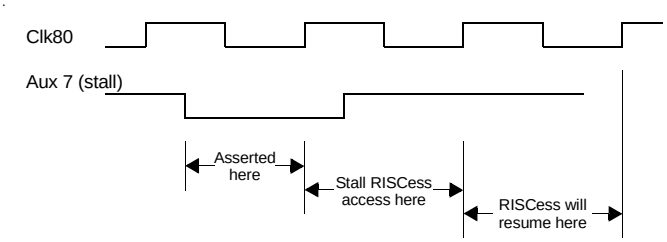
This register is a second general-purpose I/O port with four tri-state channels.

Bits	Name	Description
15:9	–	Reserved.
8	AUX7_IS_STALL	RISC Cycle Stall.
7:4	T	Tri-stateable controls.
3:0	P	Tri-stateable pads.

When this register is read, the values read are the values at the pin. Default values for tri-state controls are 0 (tri-state) at reset.

AUX7_IS_Stall Flag Operation:

The ESS RISC can be stalled externally via the AUX7 port. To configure this port, the AUX7_IS_STALL flag must be set in the RIFACE_AUX2 register (this flag defaults to 0). When set, the AUX7 (P7) pin loses its AUX pin functionality, and becomes the RISC STALL# pin. STALL# is asserted active-low, prior to the rising edge of DCI_CLK. The ESS RISC will be stalled the NEXT cycle.



For busy-holdoff operations where the ESS RISC is accessing a microprocessor which is not ready yet, the external device cannot be accessed during a zero wait state condition, since there is a 1-cycle latency before the stall can take effect.

Bus Controller (Video Processor) Registers

This section describes the Video Processor registers of the Bus Controller module in detail.

BUSCON_VP_CONTROL (0x20008000h, R/W)

—	DVE_108	LOAD_VP	VP_RST#
15:3	2	1	0

Bits	Name	Description
15:3	—	Reserved.
2	DVE_108	Video PLL Frequency Select. 1 = 108 MHz frequency selected. 0 = 54 MHz frequency selected (default).

Bits	Name	Description
1	LOAD_VP	Load Vision Processor Microcode. 1 = Load microcode.
0	VP_RST#	Vision Processor Reset. 1 = Enabled. 0 = Reset.

BUSCON_VP_STATUS (0x20008004h, R)

—	SEQ	TRD	IOSM	CMDQ_ST
15:5	4	3	2	1:0

Bits	Name	Description
15:5	—	Reserved.
4	SEQ	Sequencer Status.
3	TRD	Transfer Ready Status.
2	IOSM	I/O State Machine Status.
1:0	CMDQ_ST	Command Queue Status.

Bus Controller (Memory Controller) Registers

This section describes the Memory Controller registers of the Bus Controller module in detail.

BUSCON_DRAM_CONTROL (0x20008100h, R/W)

—	SEL SCLKEN	SD64M	SD8 BIT	BIG EDO	SD CF	SREF EN	REF EN	—	RAS PRE	RAS DEL	SPD EDO
31:17	16	15	14	13	12:11	10	9	8:6	5:4	3:2	1:0

This is the configuration register for the reference memory. After reset, it is initialized to 0x0000.

Bits	Name	Description
31:17	—	Reserved.
16	SEL SCLK EN	SDRAM Clock Enable. 1 = Pin 70 is SDSCLKEN 0 = Pin 70 is DOE#
15	SD64M	SDRAM Type Select. 1 = Use 64 Mb SDRAM 0 = Use 16 Mb SDRAM
14	SD8 BIT	SDRAM 8-Bit Select. 1 = SDRAM is x 8. 0 = SDRAM is x 16.
13	BIG EDO	EDO DRAM Select. 1 = EDO is 1M x 16 0 = EDO is 256K x 16
12:11	SDCF	SDRAM/EDO Memory Configuration.

Size (MB)	SD 64M	SD8 BIT	SD CFG1	SD CFG0	Memory Configuration
2.0	0	0	0	1	1 pc: 512Kx16x2 (16 Mb)
4.0	0	0	0	0	2 pc: 512Kx16x2 (16 Mb)
4.0	0	1	0	1	2 pc: 1Mx8x2 (16 Mb)
8.0	0	1	0	0	4 pc: 1Mx8x2 (16 Mb)
8.0	1	0	X	X	1 pc: 1Mx16x4 (64 Mb)
16.0	1	0	X	X	2 pc: 1Mx16x4 (64 Mb)
16.0	1	1	X	X	2 pc: 2Mx8x4 (64 Mb)
16.0	1	1	X	X	1 pc: 2Mx16x4 (128 Mb)

10	SREF EN	SDRAM Refresh Enable. 1 = Refresh logic for SDRAM enabled.
9	REF EN	EDO Refresh Enable. 1 = Refresh logic for EDO DRAM enabled.
8:6	—	Reserved.
5:4	RAS PRE	RAS Precharge Time Control for EDO.
3:2	RAS DEL	RAS to CAS Delay Time.
1:0	SPD EDO	EDO DRAM Speed Select.

BUSCON_DRAM_SREFTIME (0x20008114h, R/W)

INTVAL
7:0

This register controls the SDRAM refresh period for the system, and contains the refresh interval value. After reset, it is not initialized.

Bits	Name	Description
7:0	intval	SDRAM refresh interval value.

Bus Controller (Command Queue) Registers

This section describes the Command Queue registers of the Bus Controller module in detail.

BUSCON_CMDQUE_ VPDMASETUP (0x20008200h, W)

—	BK	DIR	HINT	DWS	DB	WX	DWS	DELY	DELX
31:25	24	23	22	20	19	18	17:16	15:9	8:0

The BUSCON_CMDQUE_VPDMASETUP register takes the video processor DMA access requests directed to the command queue and prioritizes the DMA requests.**Audio Registers**

Bits	Name	Description
31:25	—	Reserved.
23	BK	Break. When set, this bit sends the BREAK# signal to the VP at the end of a line.
23	DIR	Data Transfer Direction. 1 = Memory to VP. 0 = VP to memory.
22	HINT	VP Hint Block. When set, this bit blocks the DMA arbitration to the extent that the next VP DMA request will be granted over requests at the same level or below the current request level for a back-to-back VP DMA transaction.
20	DWS	Select DMA Width Enable. 1 = DMA Width Select feature enabled. 0 = Disabled.
19	DB	Double DMA Width Select. 1 = Double DMA width selected. 0 = Single DMA width selected.
18	WX	Select Delta X as DMA Width Register. 1 = Use DMA Width register. 0 = Use DELX as DMA Width register.
17:16	DSEL	DMA Width Register Select. This 2-bit field permits the selection of up to one of eight possible DMA width registers, depending on the DMA width selected by DB bit (bit 19) of this register. Four single DMA width registers and four double DMA width registers are available to support the desired DMAs for the memory configuration implemented in the design.
15:9	DELY	Transfer Y Longwords
8:0	DELX	Transfer X Scan Lines.

Audio Interface Registers

This section describes all the registers controlling the audio section, and serves as a reference for both hardware and firmware engineers who need to understand the internal workings of the Vibratto.

AUDIOCTL (0x2000D008h, R/W)

AIEN	AMS	AREN	AXEN	ABEN	DM	SRST	—
7	6	5	4	3	2	1	0

This Audio Control register enables the corresponding functions and clocks. After reset, it is initialized to 0x00.

Bits	Name	Description
7	AIEN	Audio interrupt enable. The corresponding port must be enabled for proper interrupt status. 0 = disabled. 1 = enabled.
6	AMS	Audio master clock selection: 0 = external MCLK. 1 = internal MCLK.
5	AREN	Audio receive enable. 0 = disabled. 1 = enabled.
4	AXEN	Audio transmit enable. The DMA must be started before enabling the transmit port. 1 = Audio transmit enabled. 0 = Audio transmit disabled.
3	ABEN	Audio bit clock generator enable (used only when internal MCLK is selected).
2	DM	Data input (either from pri_bus or risc) debug mode: 0 = data from pri_bus. 1 = data from risc_bus.
1	SRST	Soft reset, this bit will self-reset when a “1” is written.
0	—	Reserved.

AUDIOXMT **(0x2000D00Ch, R/W)**

TLSB	TDGE	TDFS	TDM	TCF	TFM	ITFS	TBCS	AM	TBCF
15	14	13	12:10	9:8	7:6	5	4	3:2	1:0

This Audio Transmit Format register is used for setting up the format for the transmit port. After reset, the register is initialized to 0x0000.

Bits	Name	Description
15	TLSB	Transmit LSB Select. 1 = LSB first. 0 = MSB first.
14	TDGE	Transmit Bit Clock Edge Select. 1 = output data on falling edge of clock. 0 = output data on rising edge of clock.
13	TDFS	Transmit Data Frame Sequence Select. 1 = Last bit sent on last cycle. 0 = First bit sent on first cycle.
12:10	TDM	Transmit Data Frame Mode Select. 000 = 16-bit data frame. 001 = 18-bit data frame. 010 = 20-bit data frame. 011 = 24-bit data frame. 100 = 32-bit data frame. 101 = reserved. 110 = reserved. 111 = reserved.
9:8	TCF	Transmit Cycle Frame. 00 = 16-bit cycle frame. 01 = 24-bit cycle frame. 10 = 32-bit cycle frame. 11 = reserved.
7:6	TFM	Transmit Frame Mode 00 = normal mode. 01 = Left justified mode. 10 = Right justified mode. 11 = Reserved.
5	ITFS	Inverse audio transmit frame sync. 1 = enabled. 0 = disabled.
4	TBCS	Audio Bit Clock Select 1 = use internal bit clock and output bit clock. 0 = use external bit clock.
3:2	AM	Audio Mode Select 00 = Stereo L-R channel. 01 = Dolby™ Digital (5.1 channel). 10 = MPEG-2 audio (7.1 channel). 11 = Reserved.
1:0	TBCF	Audio Transmit Bit Clock Frequency Select 00 = MCLK/8. 01 = MCLK/4. 10 = MCLK/2. 11 = MCLK/16.

AUDIORCV **(0x2000D010h, R/W)**

RLSB	RDGE	RDFS	—	RDM	RCF	RFM	RFS	RBCS	—	RBCF
15	14	13	12	11:10	9:8	7:6	5	4	3:2	1:0

This is the audio receive format register. After reset, it is initialized to 0x0000.

Bits	Name	Description
15	RLSB	Receive LSB Select. 1 = LSB first. 0 = MSB first.
14	RDGE	Receive Data Bit Clock Edge Select. 1 = Input data sampled on falling edge 0 = Input data sampled on rising edge.
13	RDFS	Receive Data Frame Sequence. 1 = Last bit sent on last cycle 0 = First bit sent on first cycle.
11:10	RDM	Receive Data Frame Select 00 = 16-bit data frame. 01 = reserved. 10 = reserved. 11 = reserved.
9:8	RCF	Receive Cycle Frame Select 00 = 16-bit cycle frame. 01 = 24-bit cycle frame. 10 = Reserved. 11 = Reserved.
7:6	RFM	Receive Frame Mode Select. 00 = Normal mode. 01 = Left justified mode. 10 = Right justified mode. 11 = reserved.
5	IRFS	Inverse Receive Frame Sync Select. 1 = enabled. 0 = disabled.
4	RBCS	Receive Bit Clock Select. 1 = Use internal bit clock and output bit clock to pin. 0 = Use external bit clock.
3:2	—	Reserved.
1:0	RBCF	Receive Bit Clock Frequency Select 00 = MCLK/8. 01 = MCLK/4. 10 = MCLK/2. 11 = MCLK/1.

AUDIOAPLLM **(0x2000D014h, R/W)**

M
7:0

This register is the Analog PLL Frequency Divider register. After reset, it is initialized to 0x4Ah.

Bits	Name	Description
7:0	M	Audio frequency divider M.

AUDIOAPLLN (0x2000D018h, R/W)

FS	OD	M8	N
7	6	5	4:0

This register is the Analog PLL Frequency Multiplier register. After reset, it is initialized to 0x1Fh.

Bits	Name	Description
7	FS	Sampling Frequency Select. 1 = 384 sample frequency selected. 0 = 256 sample frequency selected.
6	OD	Output Divider.
5	M8	Bit 8 of M Divider Value.
4:0	N	Audio frequency multiplier N.

S/PDIF Interface Registers

The following describes the S/PDIF interface registers.

SPDIF_CTL (0x2000D01Ch, R/W)

—	SPDIF_RST	SPDIF_CLK	SPDIF_SFRMV	SFRMDB	0	SPDIF_OE
7	6	5:4	3	2	1	0

After reset, it is initialized to 0x00.

Bits	Name	Description
7	–	Reserved.
6	SPDIF RST	S/PDIF Soft reset.
5:4	SPDIF _CLK	S/PDIF Bit Clock Frequency Select [1:0]. 00 = SPMCLK/8 (n=8) 01 = SPMCLK/4 (n=2) 10 = SPMCLK/2 (n=4) 11 = SPMCLK/16 (n=16)
3	SPDIF SFRMV	S/PDIF Subframe Validity Select.
2	SFRM _DB	User data bit for subframe.
1	—	Reserved. Always 0.
0	B0	SPDIF output enable: 1 = Enabled. 0 = Disabled.

SPDIF_CSD1:6 (0x2000D020h:0x2000D034h, R/W)

CDS1:6
31:0

This register is the SPDIF Channel Status 1 register. After reset, it is initialized to 0x0000 0000.

Bits	Name	Description
31:0	CDS1:6	SPDIF channel status data.

AUDIOIMASK (0x2000D038h, R/W)

MSSE	MSCSE	MSTRE	MSUE	MACS	MAUE	MATRE	MADW
7	6	5	4	3	2	1	0

This register is the Audio Interrupt Mask register. After reset, it is initialized to 0x00. Write a “1” to the corresponding bit to mask the interrupt.

Bits	Name	Description
7	MSSE	Mask for SPDIF channel swap error.
6	MSCSE	Mask for SPDIF channel status empty.
5	MSTRE	Mask for SPDIF transmit register empty.
4	MSUE	Mask for SPDIF underflow error.
3	MACS	Mask for audio channel swap error.
2	MAUE	Mask for audio underflow error.
1	MATRE	Mask for audio transmit register empty.
0	MADW	Mask for audio data waiting interrupt.

TDM Interface Registers

TDMDATA (0x2000E000h, R/W)

TDM DATA
15:0

The TDM Data register functions as a container for 16-bit data I/O transfers over the TDM port.

Bits	Name	Description
15:0	TDM DATA	TDM data transferred to and from the TDM port.

TDMXMTDELAY **(0x2000E004h, R/W)**

—	XMTDELAY	XMT_PHASE DELAY
7:4	3:1	0

This register allows a variable delay from the start of frame sync to the start of valid data (for data transmitted from RISC to TDM).

Bits	Name	Description
7:4	–	Reserved.
3:1	XMT DELAY	Transmit Delay value in milliseconds.
0	XMT PHASE DELAY	Transmit Phase delay. 1 = Normal operation. 0 = Invalid.

TDMRCVDELAY **(0x2000E008h, R/W)**

—	RCV DELAY	RCV PHASE DELAY
7:4	3:1	0

This register allows a variable delay from the start of frame sync to the start of valid data (for data transmitted from TDM to RISC).

Bits	Name	Description
7:4	–	Reserved.
3:1	RCV DELAY	Receive Delay value in milliseconds.
0	RCV PHASE DELAY	Receive Phase delay. 1 = Normal operation. 0 = Invalid.

SDRAM READ AND WRITE TIMING DIAGRAMS

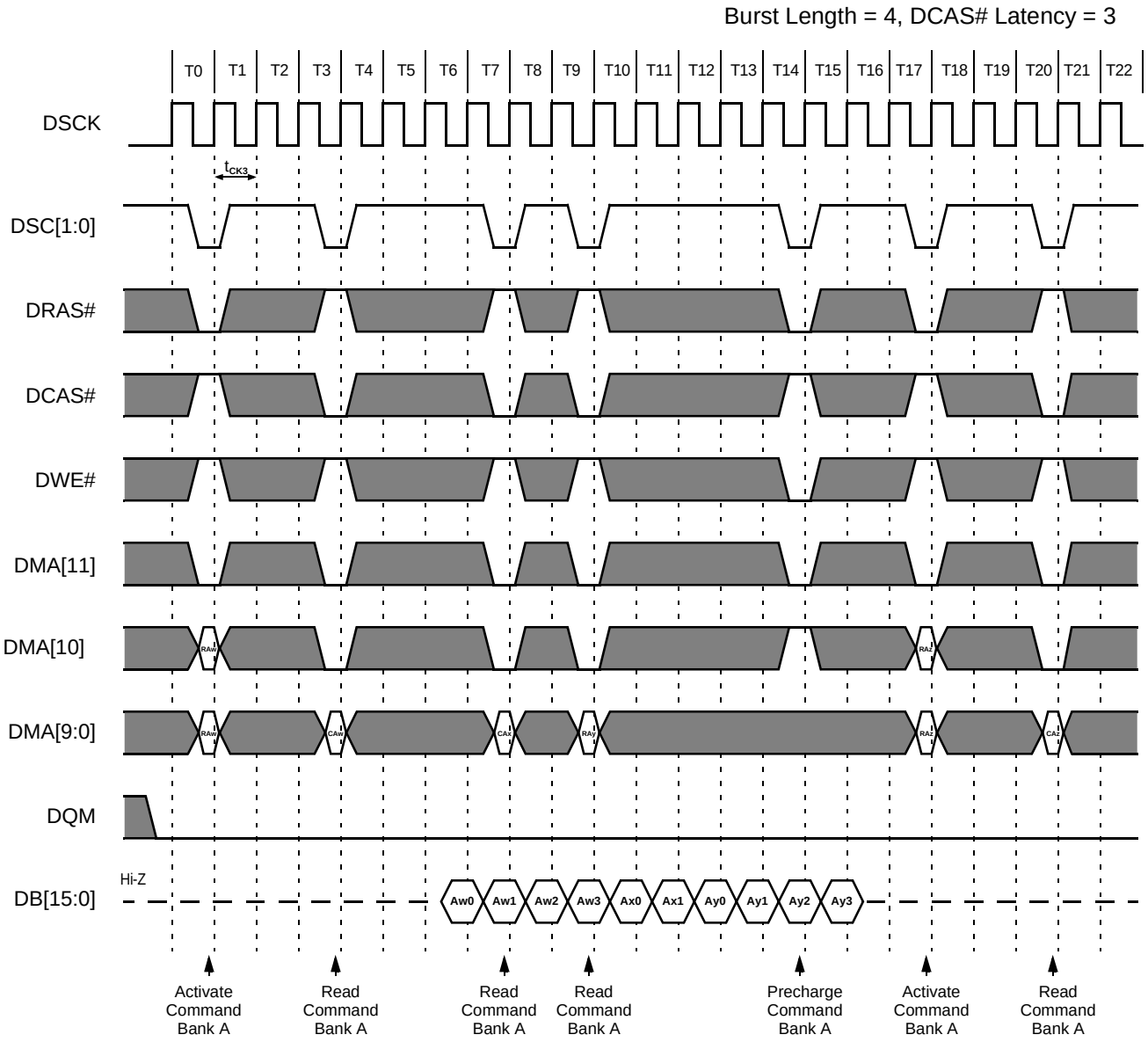


Figure 14 SDRAM Random Column Read Timing

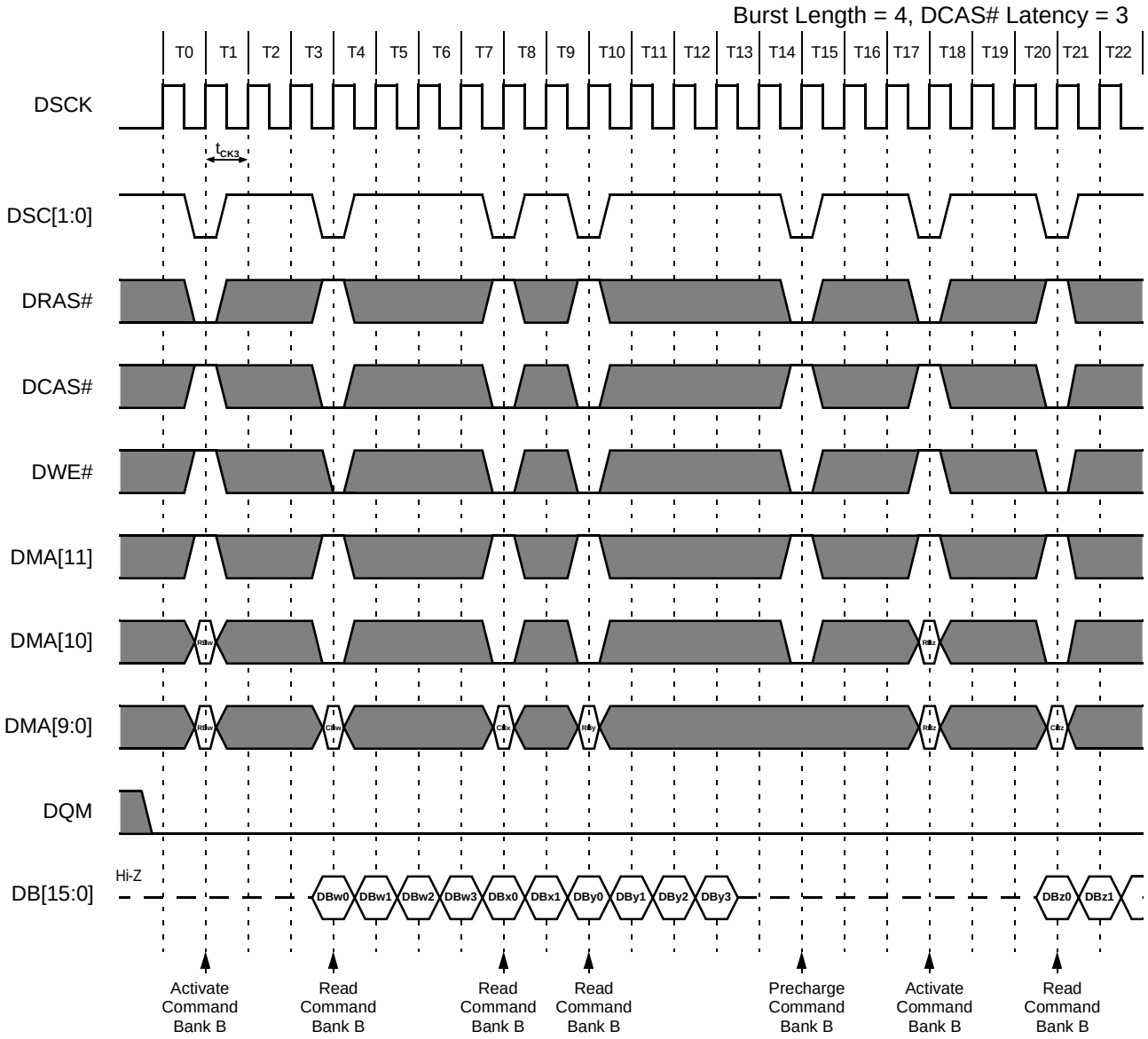


Figure 15 SDRAM Random Column Write Timing

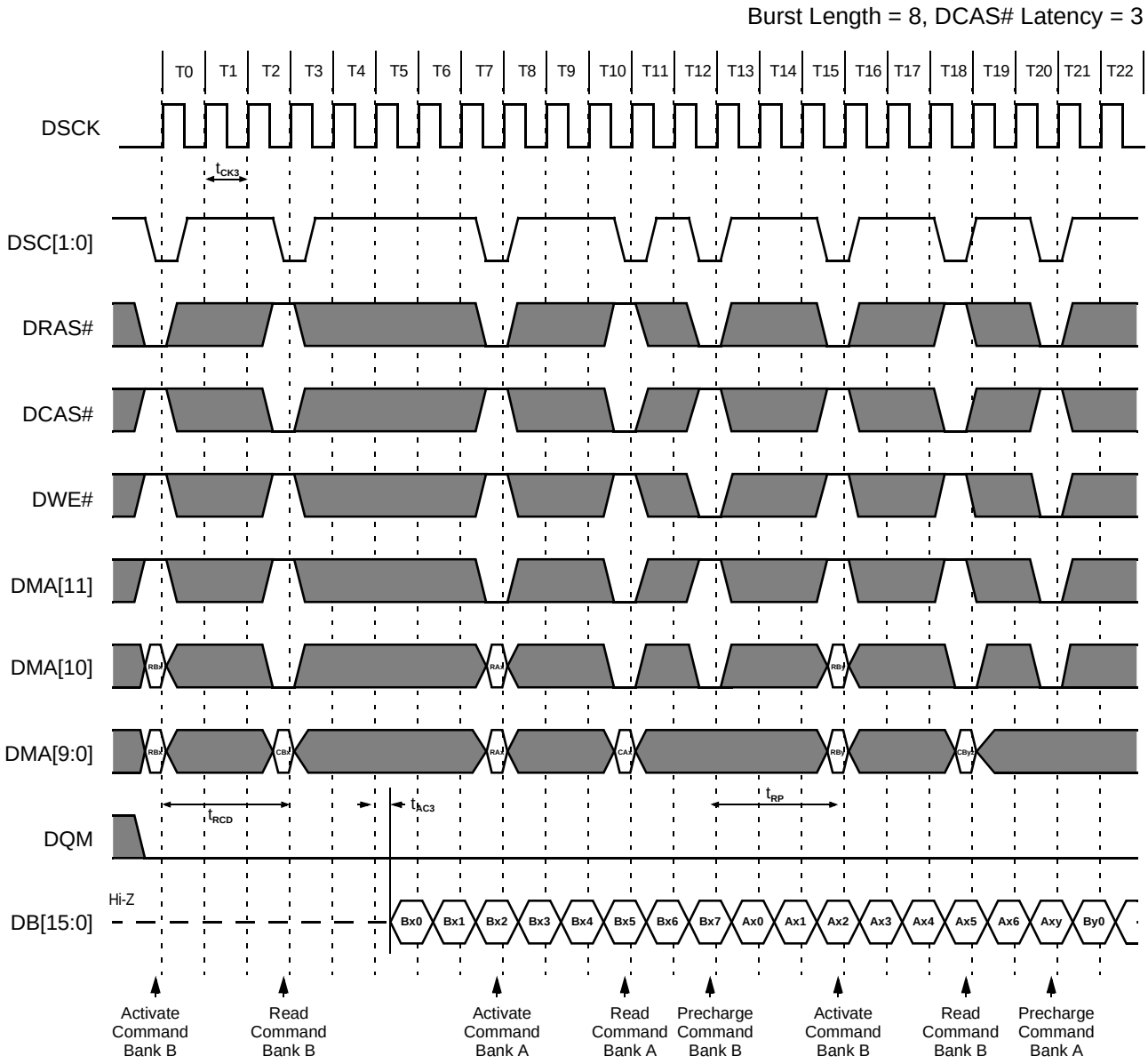


Figure 16 SDRAM Random Row Read Timing

Burst Length = 8, $\overline{CAS}$ Latency = 3

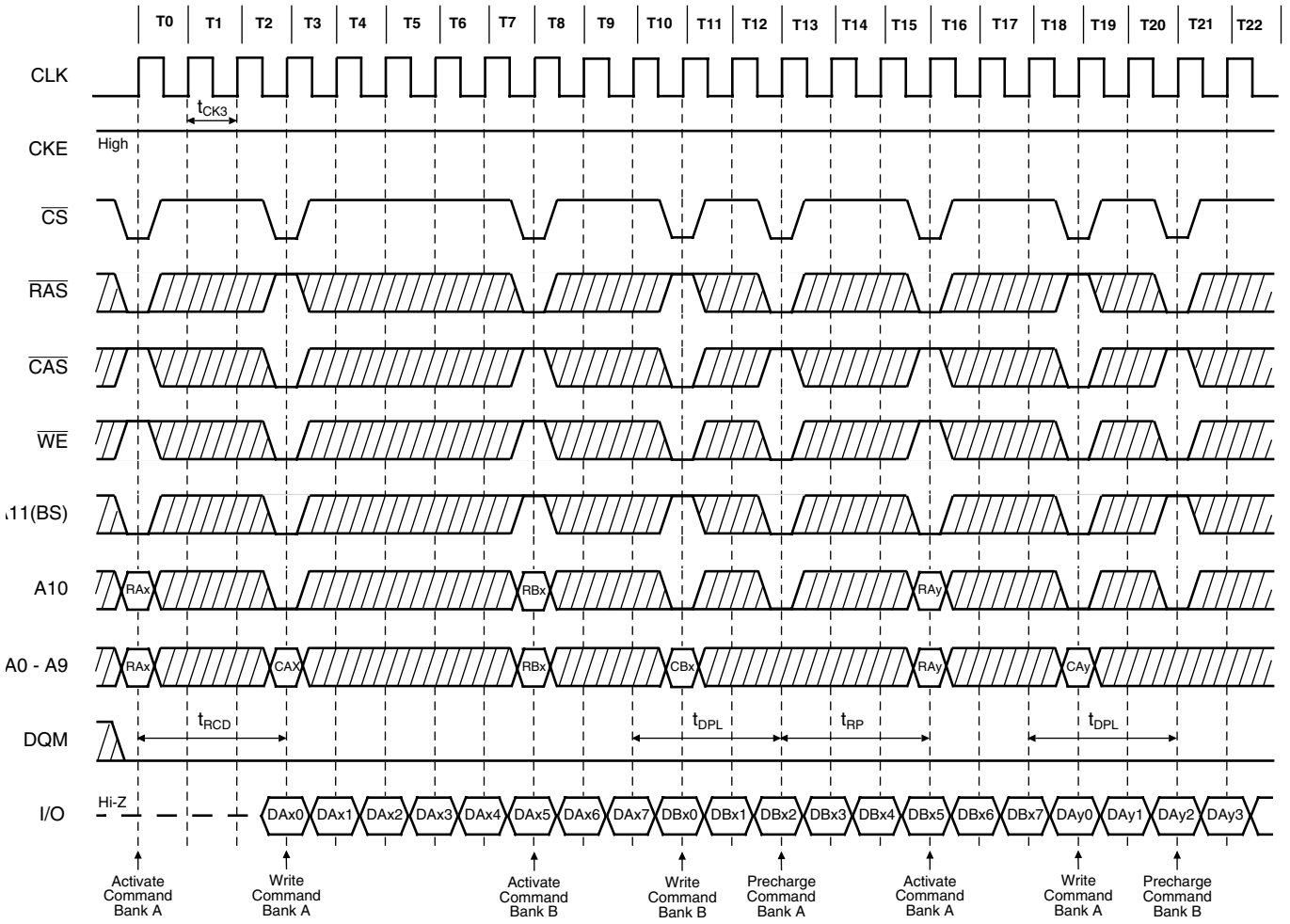


Figure 17 SDRAM Random Row Write Timing

Table 16 SDRAM Interface Timing

Parameter	Symbol	Min.	Max.	Unit	Note
Row active to Row Active Delay	t_{RRD} (min)	18		ns	1
DRAS# to DCAS# Delay	t_{RCD} (min)	24		ns	1
Row precharge time	t_{RP} (min)	24		ns	1
Row active time	t_{RAS} (min)	54		ns	1
	t_{RAS} (max)		100	µs	
Row cycle time	t_{RC} (min)	90		ns	1
Last data in to new column address delay	t_{CDL} (min)	1		CLK	2
Last data in to row precharge	t_{RDL} (min)	1		CLK	2
Last data in to burst stop	t_{BDL} (min)	1		CLK	2
Column address to column address delay	t_{CCD} (min)	1		CLK	3
Number of valid output data (CAS latency =3)		2		ea	4

Notes:

1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time, and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.

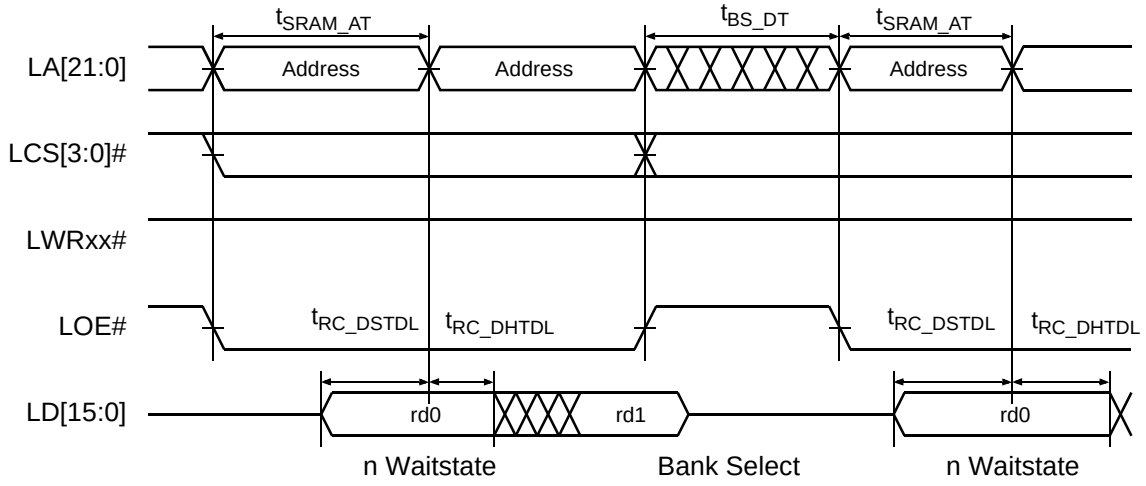
Table 17 Operating AC Characteristics

Parameter (CAS Latency = 3)	Symbol	Min.	Max.	Unit	Note
CLK cycle time	t_{CC}	9		ns	1
CLK to valid output delay	t_{SAC}		7	ns	1, 2
Output data hold time	t_{OH}	2.5		ns	2
CLK high pulse width	t_{CH}	3		ns	3
CLK low pulse width	t_{CL}	3		ns	3
Input setup time	t_{SS}	2		ns	3
Input hold time	t_{SH}	0.5		ns	3
CLK to output in low-Z	t_{SLZ}	1		ns	2
CLK to output in Hi-Z	t_{SHZ}		7	ns	

Notes:

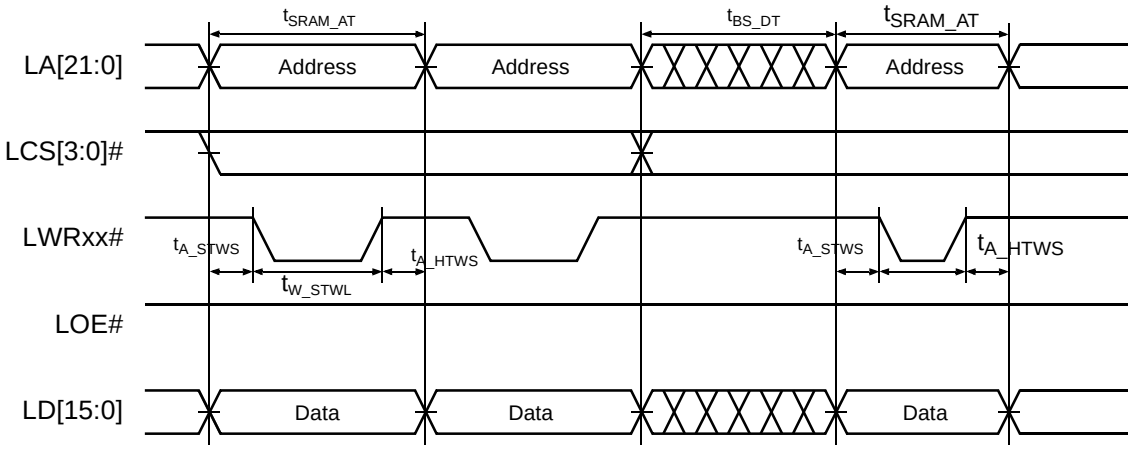
1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1 ns, (tr/2-0.5) ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf) = 1ns. If tr & tf is longer than 1 ns, transient time compensation should be considered, that is, [(tr + tf)/2 - 1] ns should be added to the parameter.

SRAM INTERFACE TIMING



Symbol	Parameter	Min	Typ	Max	Units
t_{DRAM_IOSS}	DRAM interface output signal skew	0		3	ns
t_{RC_DSTDL}	Read cycle data setup time to data latch	6		–	ns
t_{RC_DHTDL}	Read cycle data hold time to data latch	2		–	ns
t_{SRAM_AT}	SRAM access time	2*		33	internal CPU clock cycle
t_{BS_DT}	Bank Select delay time	0		3	internal CPU clock cycle

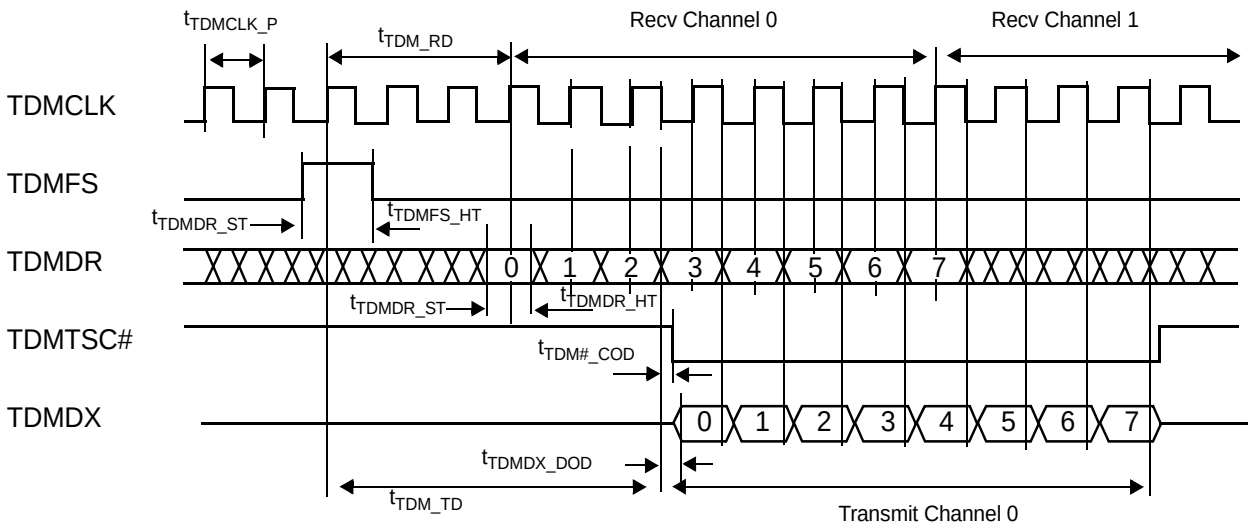
Figure 18 SRAM Read Timing



Symbol	Parameter	Min	Typ	Max	Units
t_{SRAM_IOSS}	SRAM interface output signal skew	0		3	ns
t_{SRAM_AT}	SRAM access time	2*		33	internal CPU clock cycle
t_{BS_DT}	Bank Select delay time	0		3	internal CPU clock cycle
t_{A_STWS}	Address setup time to write strobe	0.5		0.5	internal CPU clock cycle
t_{A_HTWS}	Address hold time to write strobe	0.5		0.5	internal CPU clock cycle
t_{W_STWL}	Write strobe pulse width low	1		31.5	internal CPU clock cycle

Figure 19 SRAM Write Timing

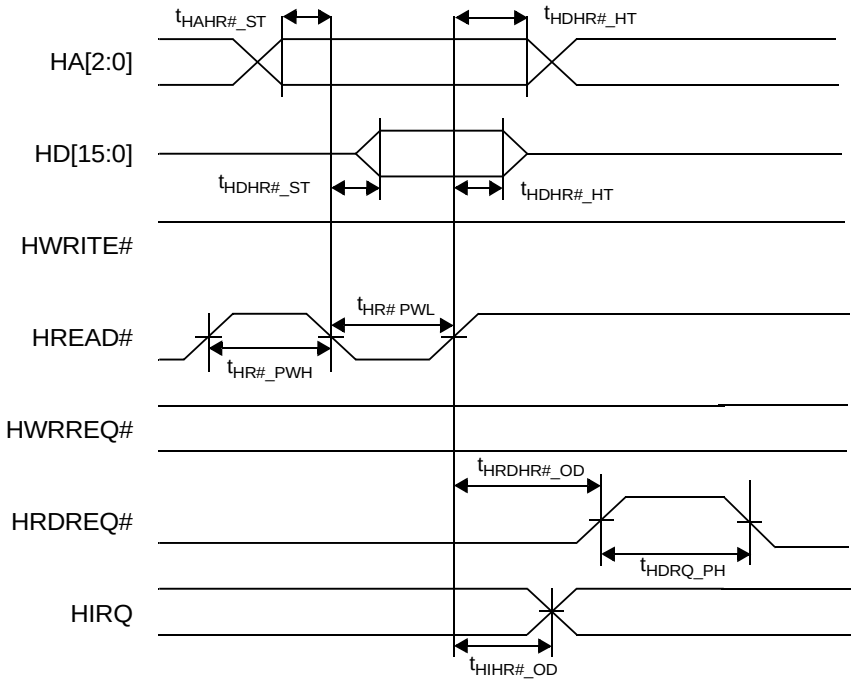
TDM INTERFACE TIMING



Symbol	Parameter	Min	Typ	Max	Units
t_{TDMCLK_P}	TDM clock period	62.5		–	ns
$t_{TDM\#\_COD}$	TDMTSC# control output delay to TDMCLK	0		2	
t_{TDMFS_ST}	TDMFS setup time to TDMCLK	4		–	
t_{TDMFS_HT}	TDMFS hold time to TDMCLK	2		–	
t_{TDMDR_ST}	TDMDR data setup time to TDMCLK	4		–	
t_{TDMDR_HT}	TDMDR data hold time to TDMCLK	2		–	
t_{TDMDX_DOD}	TDMDX data output delay to TDMCLK	0		2	
t_{TDM_RD}	TDM receive delay to TDMFS	0		8	internal CPU clock cycle
t_{TDM_TD}	TDM transmit delay to TDMFS	0		8	internal CPU clock cycle

Figure 20 TDM Interface Timing

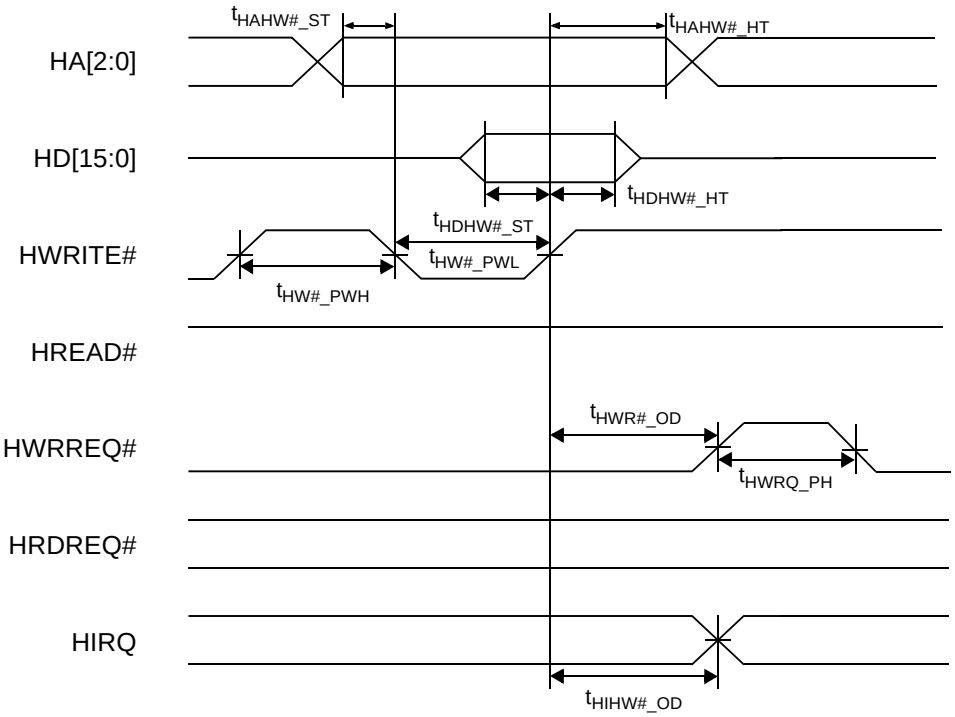
HOST INTERFACE TIMING



Symbol	Parameter	Min	Typ	Max	Units
$t_{HAHR\#\_ST}$	HA to HREAD# setup time	4		–	ns
$t_{HAHR\#\_HT}$	HA to HREAD# hold time	2		–	ns
$t_{HDHR\#\_ST}$	HD to HREAD# setup time	0		4	ns
$t_{HDHR\#\_HT}$	HD to HREAD# hold time	2		–	ns
$t_{HR\#\_PWH}$	HREAD# pulse width high	30		–	ns
$t_{HR\#\ PWL}$	HREAD# pulse width low	30		–	ns
$t_{HRDHR\#\_OD}$	HRDREQ# to HREAD# output delay	0		8	ns
$t_{HIHR\#\_OD}$	HIRQ to HREAD# output delay	0		8	ns
t_{HDRQ_PH}	HDREQ# pulse width high (See note)	75			ns

NOTE : HDREQ# is defined as a minimum value.

Figure 21 Host Bus Read Timing

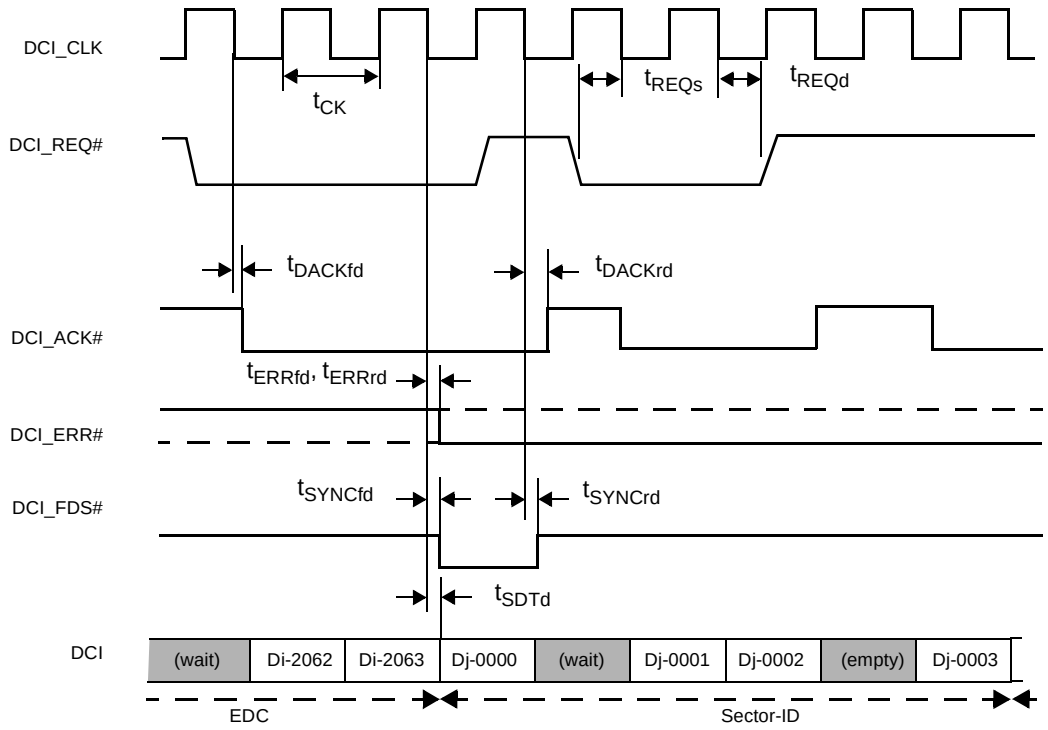


Symbol	Parameter	Min	Typ	Max	Unit
$t_{HAHW\#\_ST}$	HA to HWRITE# setup time	4		–	ns
$t_{HAHW\#\_HT}$	HA to HWRITE# hold time	2		–	ns
$t_{HDHW\#\_ST}$	HD to HWRITE# setup time	4		–	ns
$t_{HDHW\#\_HT}$	HD to HWRITE# hold time	2		–	ns
$t_{HW\#\_PWL}$	HWRITE# pulse width low	30		–	ns
$t_{HW\#\_PWH}$	HWRITE# pulse width high	30		–	ns
$t_{HWR\#\_OD}$	HWRREQ# to HWRITE# output delay	0		8	ns
$t_{HIHW\#\_OD}$	HIRQ to HWRITE# output delay	0		8	ns
t_{HWRQ_PH}	HWRREQ# pulse width high (See note)	75			ns

NOTE : HWRREQ# is defined as a minimum value.

Figure 22 Host Bus Write Timing

DCI TIMING



Symbol	Parameter	Min	Typ	Max	Units
t_{CK}	CSTROBE output frequency		3.375		MHz
t_{REQs}	REQUEST setup time	100			ns
t_{REQh}	REQUEST hold time	0			ns
t_{DACKrd}	DACK rising edge delay	0		5	ns
t_{DACKfd}	DACK falling edge delay	0		5	ns
t_{ERRrd}	ERROR rising edge delay	0		5	ns
t_{ERRfd}	ERROR falling edge delay	0		5	ns
t_{SYNCrd}	SYNC rising edge delay	0		5	ns
t_{SYNCfd}	SYNC falling edge delay	0		5	ns
t_{SDTd}	SDT[7:0] delay time	0		5	ns

Figure 23 DCI Interface Timing

AUDIO TRANSMIT AND RECEIVE TIMING DIAGRAMS

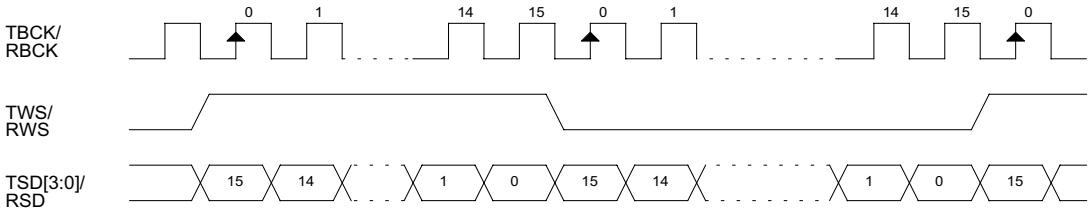


Figure 24 Right Justified Mode / 16-Bit Cycle Frame / 16-Bit Data Frame / MSB first

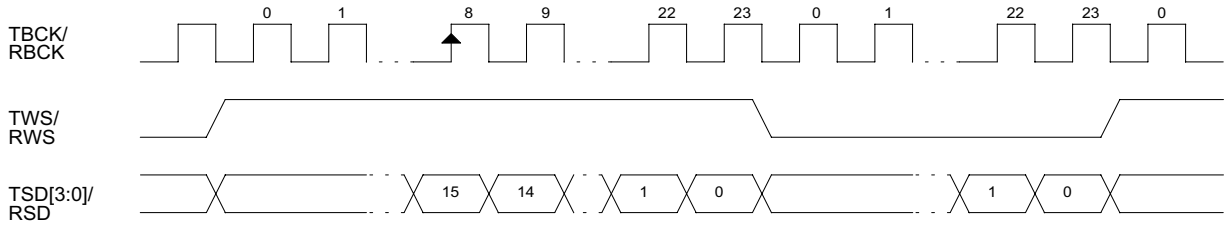


Figure 25 Right Justified Mode / 24-Bit Cycle Frame / 16-Bit Data Frame / MSB First

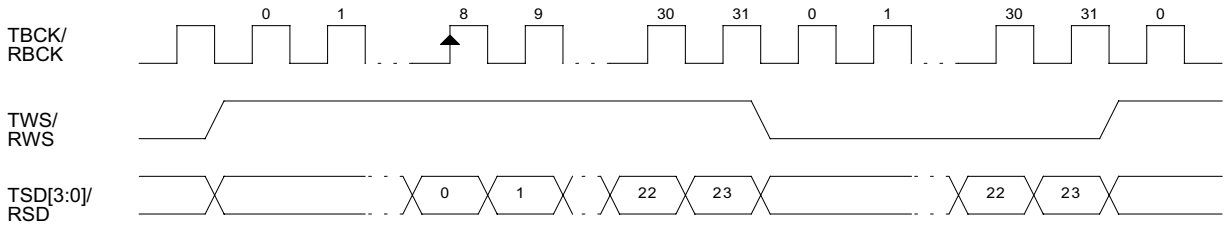


Figure 26 Right Justified Mode / 32-Bit Cycle Frame / 24-Bit Data Frame / LSB First

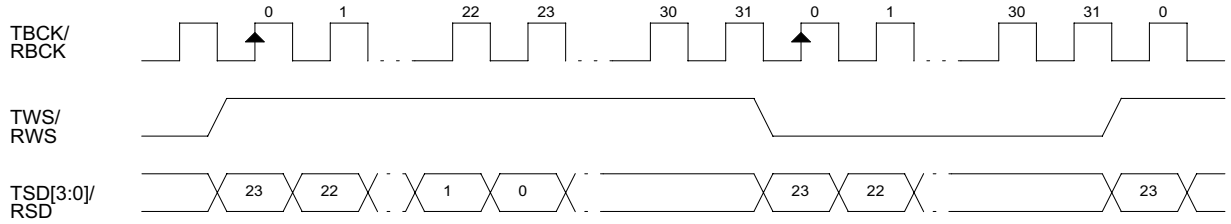


Figure 27 Left Justified Mode / 32-Bit Cycle Frame / 24-Bit Data Frame / MSB First

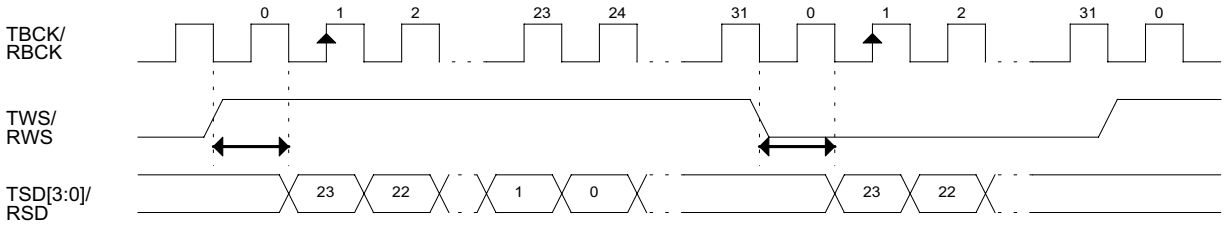


Figure 28 I²S Mode

VIDEO TIMING DIAGRAMS

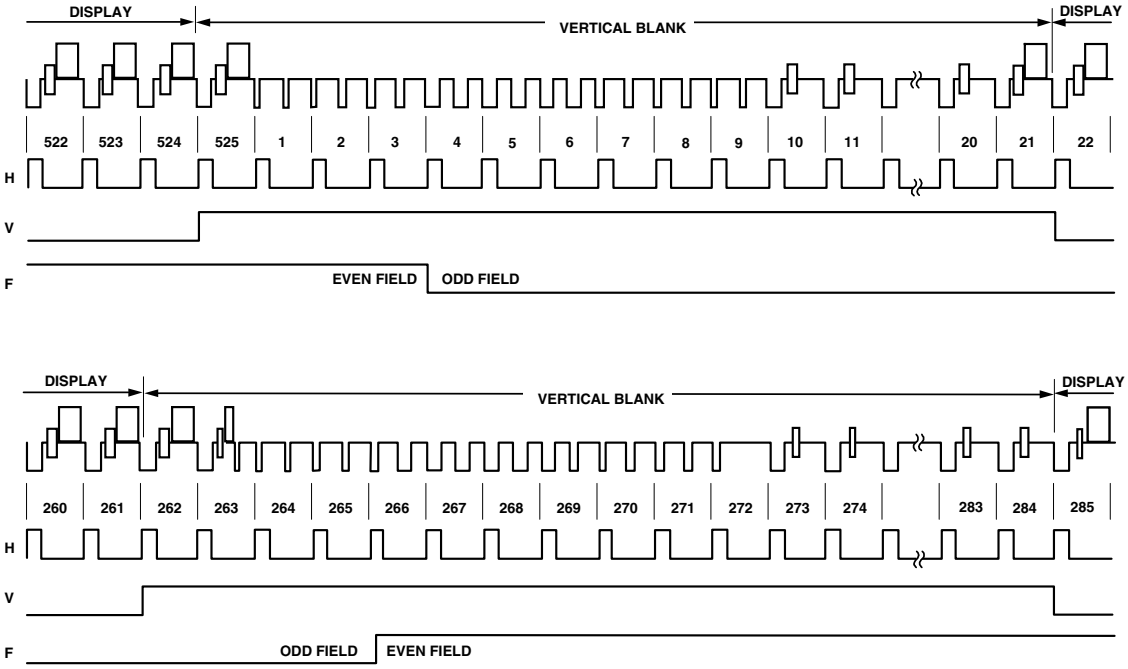


Figure 29 NTSC Timing

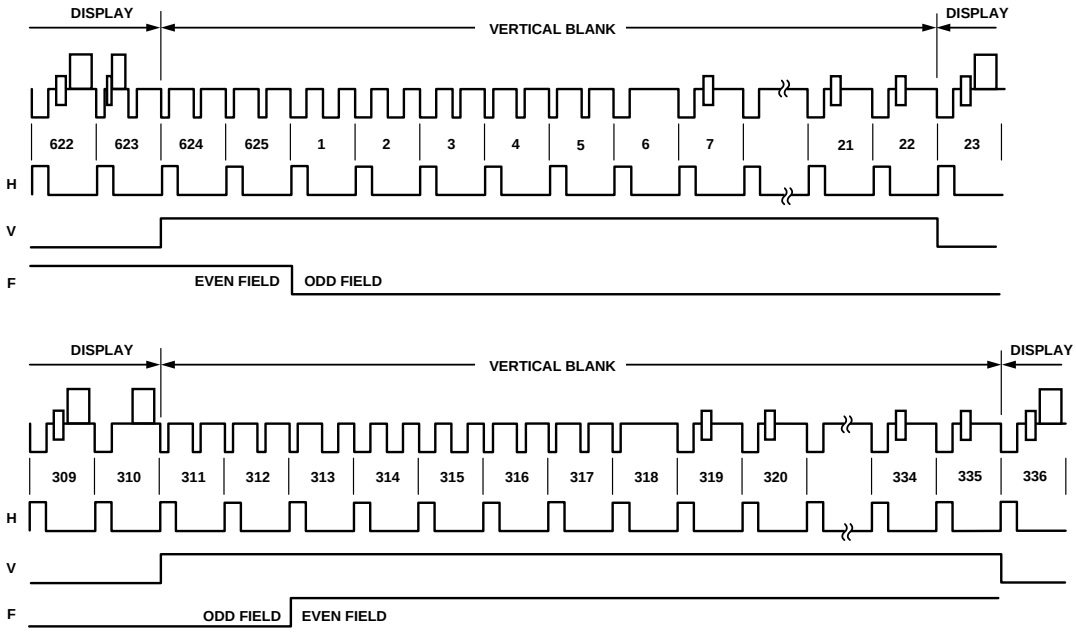


Figure 30 PAL Timing

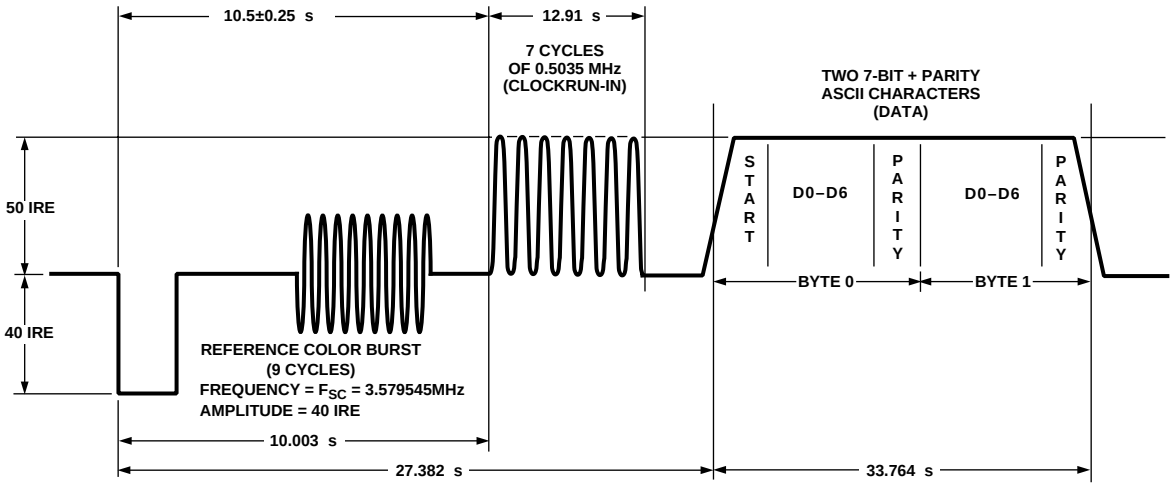


Figure 31 NTSC Closed Captioning Timing

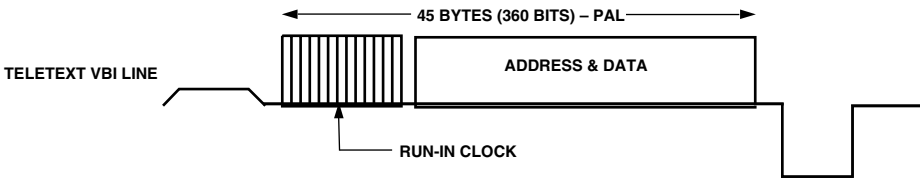


Figure 32 PAL Teletext / Vertical Blanking Interval Timing

PREAMBLE ADDRESS CODES

	Row 1	Row 2	Row 3	Row 4	Row 5	Row 6	Row 7	Row 8	Row 9	Row 10	Row 11	Row 12	Row 13	Row 14	Row 15
First byte of code pair:															
Data Channel 1	11	11	12	12	15	15	16	16	17	17	10	13	13	14	14
Data Channel 2	19	19	1A	1A	1D	1D	1E	1E	1F	1F	18	1B	1B	1C	1C
Second byte of code pair:															
White	40	60	40	60	40	60	40	60	40	60	40	40	60	40	60
White Underline	41	61	41	61	41	61	41	61	41	61	41	41	61	41	61
Green	42	62	42	62	42	62	42	62	42	62	42	42	62	42	62
Green Underline	43	63	43	63	43	63	43	63	43	63	43	43	63	43	63
Blue	44	64	44	64	44	64	44	64	44	64	44	44	64	44	64
Blue Underline	45	65	45	65	45	65	45	65	45	65	45	45	65	45	65
Cyan	46	66	46	66	46	66	46	66	46	66	46	46	66	46	66
Cyan Underline	47	67	47	67	47	67	47	67	47	67	47	47	67	47	67
Red	48	68	48	68	48	68	48	68	48	68	48	48	68	48	68
Red Underline	49	69	49	69	49	69	49	69	49	69	49	49	69	49	69
Yellow	4A	6A	4A	6A	4A	6A	4A	6A	4A	6A	4A	4A	6A	4A	6A
Yellow Underline	4B	6B	4B	6B	4B	6B	4B	6B	4B	6B	4B	4B	68	4B	6B
Magenta	4C	6C	4C	6C	4C	6C	4C	6C	4C	6C	4C	4C	6C	4C	6C
Magenta Underline	4D	6D	4D	6D	4D	6D	4D	6D	4D	6D	4D	4D	6D	4D	6D
White Italics	4E	6E	4E	6E	4E	6E	4E	6E	4E	6E	4E	4E	6E	4E	6E
White Italics Underline	4F	6F	4F	6F	4F	6F	4F	6F	4F	6F	4F	4F	6F	4F	6F
Indent 0	50	70	50	70	50	70	50	70	50	70	50	50	70	50	70
Indent 0 Underline	51	71	51	71	51	71	51	71	51	71	51	51	71	51	71
Indent 4	52	72	52	72	52	72	52	72	52	72	52	52	72	52	72
Indent 4 Underline	53	73	53	73	53	73	53	73	53	73	53	53	73	53	73
Indent 8	54	74	54	74	54	74	54	74	54	74	54	54	74	54	74
Indent 8 Underline	55	75	55	75	55	75	55	75	55	75	55	55	75	55	75
Indent 12	56	76	56	76	56	76	56	76	56	76	56	56	76	56	76
Indent 12 Underline	57	77	57	77	57	77	57	77	57	77	57	57	77	57	77
Indent 16	58	78	58	78	58	78	58	78	58	78	58	58	78	58	78
Indent 16 Underline	59	79	59	79	59	79	59	79	59	79	59	59	79	59	79
Indent 20	5A	7A	5A	7A	5A	7A	5A	7A	5A	7A	5A	5A	7A	5A	7A
Indent 20 Underline	5B	7B	5B	7B	5B	7B	5B	7B	5B	7B	5B	5B	7B	5B	7B
Indent 24	5C	7C	5C	7C	5C	7C	5C	7C	5C	7C	5C	5C	7C	5C	7C
Indent 24 Underline	5D	7D	5D	7D	5D	7D	5D	7D	5D	7D	5D	5D	7D	5D	7D
Indent 28	5E	7E	5E	7E	5E	7E	5E	7E	5E	7E	5E	5E	7E	5E	7E
Indent 28 Underline	5F	7F	5F	7F	5F	7F	5F	7F	5F	7F	5F	5F	7F	5F	7F

NOTE: All indent codes (second byte equals 50h±5fh, 70th±7fh) assign white as the color attribute.

Figure 33 Line 21 Preamble Address Codes (Same As FCC Part 15.119)

DVE NTSC SQ Simulation

Code	V	IRE
954	1.233	172.7
774	1.001	140.1
715	0.924	129.4
476	0.616	86.2
336	0.434	60.8
263	0.340	47.6
221	0.286	40.0
106	0.138	19.3
83	0.108	15.1
0	0.000	0.0

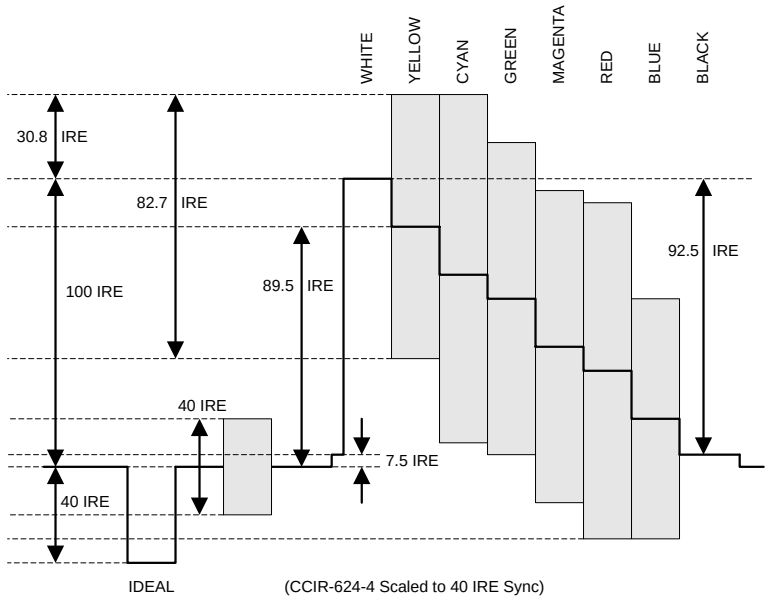


Figure 34 NTSC Composite (VDAC) Line Output Waveform

DVE PAL SQ Simulation

Code	V	IRE
960	1.241	173.8
774	1.001	140.1
712	0.921	128.9
464	0.600	84.0
349	0.451	63.1
232	0.300	42.0
115	0.149	20.8
46	0.060	8.4
0	0.000	0.0

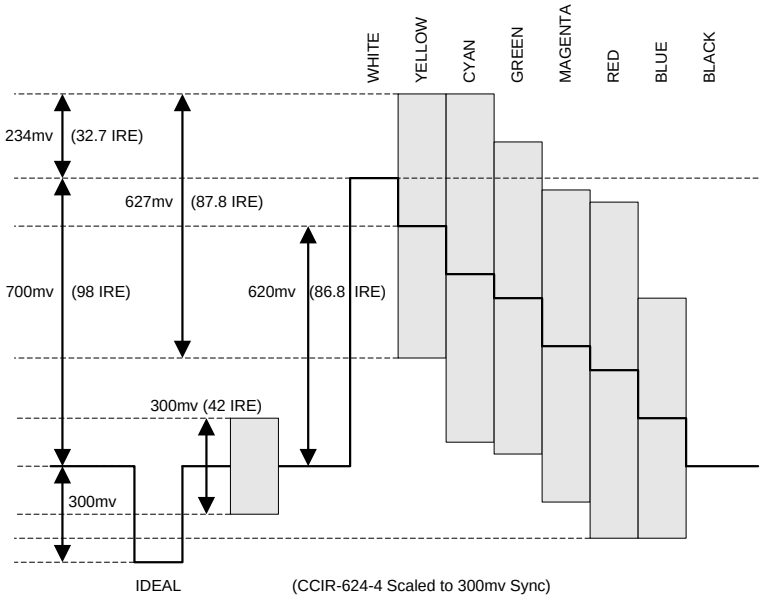


Figure 35 PAL Composite (VDAC) Line Output Waveform

DVE NTSC SQ Simulation

Code	V	IRE
387	1.001	140.1
716	0.926	129.6
620	0.802	112.2
561	0.725	101.5
476	0.615	86.2
417	0.539	75.5
322	0.416	58.3
263	0.340	47.6
221	0.286	40.0
0	0.000	0.0

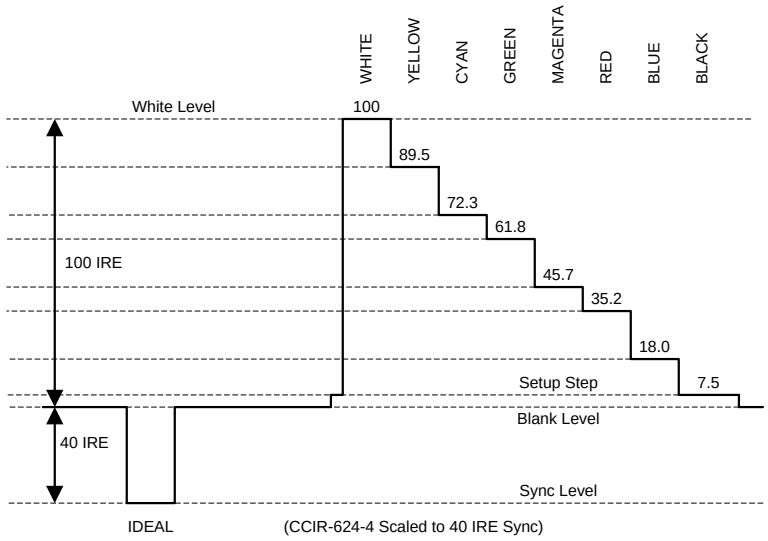
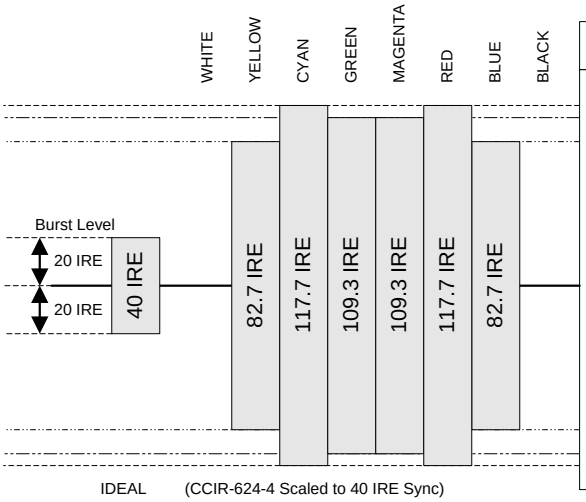


Figure 36 Luma (YDAC) Line Output Waveform

DVE NTSC SQ Simulation

Code	V	IRE
847	1.095	153.3
826	1.068	149.6
752	0.972	136.1
626	0.810	113.4
512	0.662	92.7
398	0.514	72.0
273	0.353	49.4
199	0.257	36.0
178	0.230	32.2

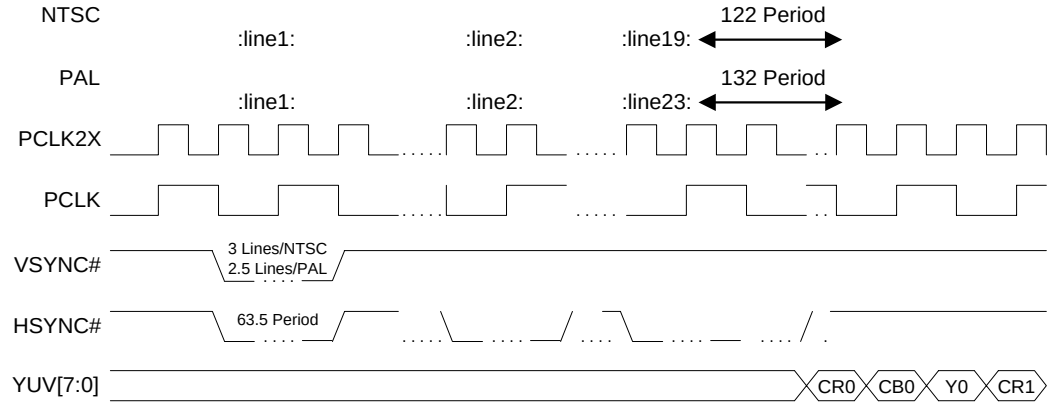


DVE NTSC SQ Simulation

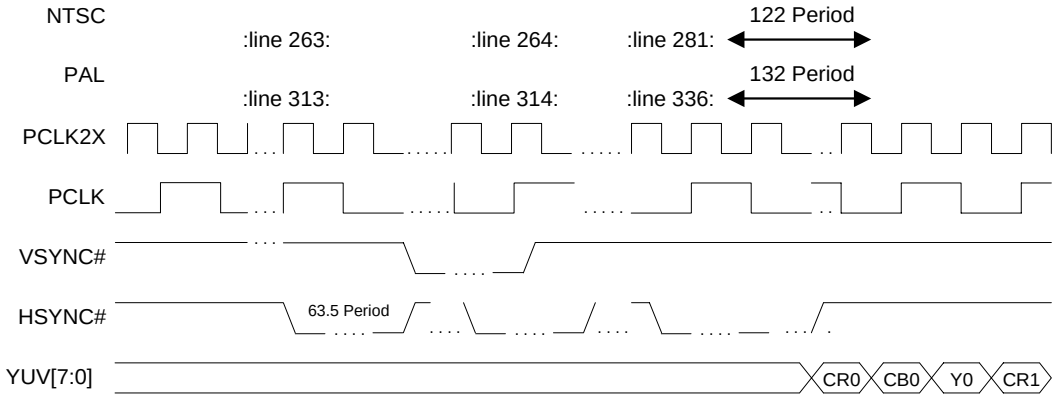
Code	V	IRE
847	1.095	153.4
827	1.069	149.7
752	0.972	136.1
512	0.662	92.7
273	0.353	49.4
199	0.257	36.0
178	0.231	32.3

Figure 37 Chroma (CDAC) Line Output Waveform

Field 1



Field 2



1 Period = 1 Pixel Clock

Figure 38 Sync and Pixel Clock Timings

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Storage temperature range	-65° C to 150° C
Operating temperature range	0° C to 70° C
Voltage range on any pin	-0.5 V to + 0.5 V
Power dissipation	1.8 W

Recommended Operating Conditions

Operating temperature range	0° C to 70° C
Supply voltage VCC	2.80V±150 mV; 375 mA nominal
Supply voltage VEE	3.60V±150 mV; 50 mA nominal
Supply voltage AVEE	3.60V±150 mV; 10 mA nominal
Supply voltage ADVEE	3.60V±150 mV; 150 mA nominal

WARNING: Stress beyond those listed under the Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the Recommended Operating Conditions section of this specification is not implied. Exposure to the Absolute Maximum Ratings conditions for extended periods may affect device reliability.

DC Electrical Characteristics

Video DAC

Parameter	Condition	Min	Typ	Max	Unit
DAC resolution		–	10	–	bits
Integral linearity	(INL)	–	±2	±2	LSB
Differential linearity error	(DNL)	–	±0.5	±1	LSB
Gain error		–	--	±5	%
DAC output impedance		–	20K	–	Ω
Output current-DAC		33.5	35.2	36.5	mA
Internal reference voltage	(V_{REF})	1.17	1.235	1.29	V
Output load		34	37.5	42	Ω
Output capacitance		–	–	40	pF

Table 18 DC Electrical Characteristics

Symbol	Parameter	Min	Max	Unit	Comments
V_{IH}	High-level input voltage	2.0	VCC+0.25	V	All inputs TTL levels except CLK
V_{IL}	Low-level input voltage	-0.3	0.8	V	All inputs TTL levels except CLK
V_{CLKH}	CLK high-level input	2.0	VCC+0.25	V	TTL level input
V_{CLKL}	CLK low-level input	-0.3	0.8	V	TTL level input
V_{OH}	High-level output voltage	3.0	–	V	I_{OH} = 1 mA
V_{OL}	Low-level output voltage	–	0.45	V	I_{OL} = 4 mA
I_{LI}	Input leakage current	–	±15	µA	
I_{LO}	Output leakage current	–	±15	µA	
C_{IN}	Input capacitance	–	10	pF	fc = 1 MHz
C_O	Input/output capacitance	–	12	pF	fc = 1 MHz
C_{CLK}	CLK capacitance	–	20	pF	fc = 1 MHz

AC Electrical Characteristics

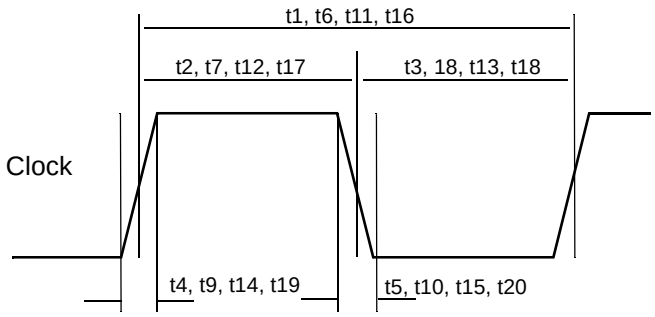


Table 19 Clock Timing Parameters

Symbol		Parameter	Min	Typ	Max	Units
Pixel Clock Timing						
t1	t_{CLK_P}	Clock period	30		100	ns
t2	t_{CLK_LT}	Clock low time	24		–	ns
t3	t_{CLK_HT}	Clock high time	24		–	ns
t4	t_{CLK_RT}	Clock rise time	–		6	ns
t5	t_{CLK_FT}	Clock fall time	–		6	ns
t6	t_{PCLK_P}	Pixel clock period	33		–	ns
Doubled Pixel Clock Timing						
t7	t_{PCLK_LT}	Pixel clock low time	15		–	ns
t8	t_{PCLK_HT}	Pixel clock high time	15		–	ns
t9	t_{PCLK_RT}	Pixel clock rise time	–		4	ns
t10	t_{PCLK_FT}	Pixel clock fall time	–		4	ns
Audio Master Clock Timing						
t11	t_{ACLK_P}	Audio clock period	54		–	ns
t12	t_{ACLK_LT}	Audio clock low time	21		–	ns
t13	t_{ACLK_HT}	Audio clock high time	21		–	ns
t14	t_{ACLK_RT}	Audio clock rise time	–		6	ns
t15	t_{ACLK_FT}	Audio clock fall time	–		6	ns
TDM Clock Timing						
t16	t_{TDMCLK_P}	TDM clock period	62.5		–	ns
t17	t_{TDMCLK_LT}	TDM clock low time	25		–	ns
t18	t_{TDMCLK_HT}	TDM clock high time	25		–	ns
t19	t_{TDMCLK_RT}	TDM clock rise time	–		6	ns
t20	t_{TDMCLK_FT}	TDM clock fall time	–		6	ns

Figure 39 Pixel, Doubled Pixel, TDM and Audio Master Clock Timing

ES60X8 DESIGN GUIDE

DVD Printed Circuit Board Layout Guidelines

About Multilayer Boards

A multilayer board with dedicated power and ground planes is recommended. The power and ground planes should be placed close together in order to increase the distributed mutual capacitance on the board. Distributing the mutual capacitance will result in the board exhibiting less crosstalk and less power supply noise, while also providing better high frequency bypass characteristics.

A good ground net should have low impedance and low inductance, as poor grounding can cause the loss of the low-level DC noise margin. Noise spikes due to long ground return paths are also possible. These noise spikes can cause false switching of sensitive strobe signals.

In some cases, the fast switching may show up as being software dependent because different combinations of 1's and 0's create different return currents in the ground net. The power net, like the ground net, should be low impedance and low inductance. A high impedance power net may cause large voltage drops, reducing the high-level noise margin.

Multilayer boards exhibit less EMI problems because of the low inductance planes. The planes reduce the size of the current loop, thus reducing the radiation area. Solid power and ground planes will help dissipate heat from devices such as voltage regulators and the Vibratto, resulting in the heat becoming redirected towards cooler areas of the board. This dissipating effect can be realized even if the device is not electrically connected to the net.

Power and Ground Planes

The ground planes should encompass all the ground pins, voltage reference circuitry, and power traces for the Vibratto, along with the analog output and digital signal traces leading to the Vibratto. Both the analog and digital sections of the Vibratto should have their own dedicated power planes, so as to reduce the possibility of plane-to-plane noise coupling.

Digital Signal Interconnect

The digital signal inputs to the Vibratto should be isolated as much as possible from the from the analog outputs and other analog output circuitry. As the Vibratto implements high clock rates, avoid long clock lines to preclude noise pickup.

Finally, active termination resistors that may be implemented for the digital inputs should be connected to the regular PCB power plane whenever possible.

Analog Signal Interconnect

The analog outputs should be isolated from the digital signals as much as possible since they are susceptible to crosstalk from the digital lines. Digital traces must not be run adjacent to or under analog lines. The distance between the analog output pin and the output connector should be kept short as possible to minimize noise pickup and reflections caused by impedance mismatch.

The load resistor for each output should be placed as close to the pin as possible to minimize reflections. The analog output signals should overlay the ground plane and not the power plane in order to maximize the high frequency power supply rejection.

Layout Considerations

All of the Vibratto DVD processors require heat sinking. To accomplish this in an economical manner, use the following PCB layout shown in Figure 40. The land pattern for the Vibratto still uses the standard 208 pin PQFP footprint.

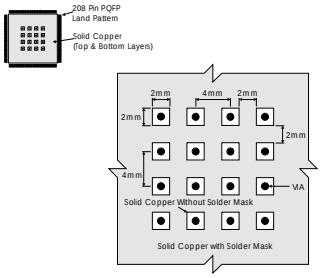


Figure 40 PCB Layout Considerations

Addition of a solid copper fill on the top and bottom layers, along with 2mm square solder mask exposures and via holes in the center of each exposure is recommended. If a multilayer board is used, the power and ground planes will act as a heat spreader, precluding the need for copper fill on the top and bottom layers.

Power Supply Decoupling

For peak performance, all bypass capacitors should be placed as close as possible to the device using the shortest leads possible. Chip capacitors are recommended for their low lead inductance. Surface mount capacitors should be placed on the component side to reduce the inductance caused by vias.

If vias must be used, the vias should be as large as possible to minimize inductance effects. A typical implementation uses 0.1µF capacitors for high-frequency noise rejection, and a 10µF to 47µF capacitor for low-

frequency ripple. To further reduce power supply ripple, place a larger capacitor, such as a 47µF to 470µF capacitor, near the power supply entry point.

Compensation Capacitor Decoupling

COMP pin 109 must be decoupled to the ADVEE supply using a surface mount 0.1µF ceramic capacitor. A surface mount capacitor is recommended because of its low lead inductance. Lead inductance reduces the ability of the circuit to reject noise. The capacitor should be placed on the component side, as close as possible to the COMP pin 109 using a short, wide trace.

Reference Voltage Decoupling

VREF pin 107 is used to decouple the internal voltage reference for the video DAC. Decouple the pin with a 0.1µF ceramic capacitor to the ground plane. Place the capacitor as close as possible to VREF pin 107 and connect the capacitor using a short, wide trace.

DAC Current Adjustment Resistor

RSET pin 110 is used to select the full scale output current of the internal video DAC. A resistor between 200 and 1000 ohms should connect between RSET pin 110 and the ground plane, depending on whether or not buffer circuitry is implemented in the board design. The resistor must be placed close to the pin and connected using a short, wide trace.

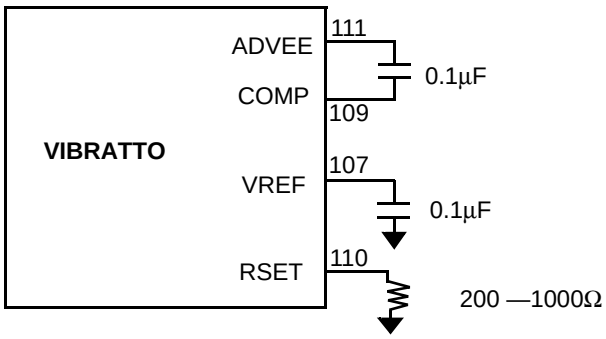


Figure 41 Typical Video DAC Connection Diagram

SDRAM Signal Routing

The SDRAM signals should be routed on the component layer if possible using the shortest trace possible. The use of vias should be kept to a minimum to reduce reflections due to discontinuities in the signal path.

When routing the SDRAM clock signal, care should be taken. This clock signal operates at the same frequency as the decoder. Additional air gap between the clock signal and other signals is recommend to reduce crosstalk.

About The Vibratto Evaluation Board

The evaluation mainboard is provided as an example of how the Vibratto DVD processor can be implemented in a DVD player design. A DVD player design can not be fully implemented using only one board. Additional boards such as A/V output, mic preamp and front panel boards are also needed. The design was done in a modular fashion so that customer-specific configurations could also be realized with this design.

Evaluation Mainboard Features

The Vibratto evaluation mainboard supports the following features:

- Playback of CD, VCD, SVCD, DVD, MP3, Kodak Picture CD, JPEG format disc media
- Analog 2-channel audio output
- Digital 6-channel audio output
- S/PDIF output
- 2-channel analog audio input
- Built-in video encoder supporting interlace and 480-pixel progressive scan outputs
- Interface to VFD front control panel
- Interface for infra-red remote control
- Direct connection to ATAPI DVD Loader
- Supports MOD X loader modules
- Supports MOD X-FLASH memory module

Boards that can be directly connected to this board include those listed in Table 20:

Table 20 Add-On DVD Player Boards and Modules

Board Name	Description
ESS DVD VFD Control	Front panel for DVD applications, VFD display, mic preamp.
ESS Avatar	6 Channel Dolby Digital output, S/PDIF optical and coax output, video filters
MOD X - Flash	Flash/SRAM Development Module
MOD X - Flash Socket	Socketed TSOP Flash Develop-ment module
MOD X - Philips	Philips Loader Interface Module
MOD X - Thomson	Thomson Loader Interface Module
MOD X - Sony	Sony Loader Interface Module
MOD X - DCI/Sanyo	DCI/Sanyo Loader Interface Module
MOD X - UDE/Panasonic	UDE/Panasonic Loader Interface Module

The Vibratto evaluation board has been designed to use the ATAPI interface and internal video encoder features of the device. All of the Vibratto DVD processors can operate at a variety of frequencies. Refer to Table 21 to set the operating frequency.

Table 21 The Vibratto Clock Frequency Matrix

SEL_PLL2	SEL_PLL1	SEL_PLL0	Multiplier
0	0	0	VCO OFF
0	0	1	1X
0	1	0	BYPASS
0	1	1	2X
1	0	0	4.5X
1	0	1	3X
1	1	0	3.5X
1	1	1	4X

The internal video encoder supports four combinations of video outputs. The outputs can be in NTSC or PAL formats. When the internal video encoder of the Vibratto is used, pin 109 becomes the compensation input, pin 107 is the bypass pin for the internal voltage reference, and pin 110 sets the full scale output current of the DACs. Table 22 lists the possible video output combinations for the Vibratto.

Table 22 Video Output Combinations Matrix

Mode	YDAC pin 113	UDAC pin 106	VDAC pin 114	CDAC pin 108
A	Y	C	COMP	C
B	Y	COMP	COMP	C
C	Y	U	COMP	V
D	Y	U	C	V

Connector Pin Assignments

Table 23 through Table 33 list the jumper pins on the Asteroid DVD demo board and the corresponding signal names.

Table 23 JS1 (DVD Drive Expansion Connector

Pin	Signal	Pin	Signal
1	+5V	2	+12V
3	VCC33	4	+12V
5	RST#	6	LD9
7	LD8	8	LD11
9	LD10	10	ISPCLK

Table 23 JS1 (DVD Drive Expansion Connector

Pin	Signal	Pin	Signal
11	LD12	12	DEMCLK
13	HWRQ#	14	RD1
15	WR2	16	TDMDR
17	TDMCLK	18	TDMFS
19	AUX0	20	AUX1
21	AUX3	22	AUX5
23	GND	24	GND

Table 24 JS2 ATAPI Interface Connector

Pin	Signal	Pin	Signal
1	RESET	2	GND
3	DD15	4	D0
5	DD14	6	D1
7	DD13	8	D2
9	DD12	10	D3
11	DD11	12	D4
13	DD10	14	D5
15	DD9	16	D6
17	DD8	18	D7
19	GND	20	KEY
21	DRQ	22	GND
23	IOW#	24	GND
25	IOR#	26	GND
27	IOCHRDY	28	BALE
29	DACK#	30	GND
31	IRQ14	32	IOCS16#
33	A1	34	Reserved
35	A0	36	A2
37	CS0#	38	CS1#
39	Activity	40	GND

Table 25 JS3 Video Connector

Pin	Signal Name	Pin	Signal Name
1	UDAC	2	CDAC
3	YDAC	4	GND
5	VDAC	6	GND
7	VSYNC#	8	HSYNC#

Table 26 JS4 Power Connector

Pin	Signal Name	Pin	Signal Name
1	+5V	2	GND
3	GND	4	+12V
5	-12V	6	GND

Table 27 JS5 VFD Interface Connector

Pin	Signal Name	Pin	Signal Name
1	+5V	2	IR
3	GND	4	VFD_CLK
5	VFD_CS	6	VFD_DATA

Table 28 JS6 S/PDIF Connector

Pin	Signal Name	Pin	Signal Name
1	TXP	2	GND
3	GND	4	TXN

Table 29 JS7 Audio Input Connector

Pin	Signal Name	Pin	Signal Name
1	MICR	2	GND
3	GND	4	MICL

Table 30 JS8 Audio Output Connector

Pin	Signal Name	Pin	Signal Name
1	ZEROR	2	RIGHT
3	GND	4	GND
5	LEFT	6	ZEROL

Table 31 JS9 Audio Board Connector

Pin	Signal Name	Pin	Signal Name
1	CLKEX	2	GND
3	TBCK	4	TSD0
5	TWS	6	TSD1
7	GND	8	TSD2
9	AUX3	10	GND
11	AUX5	12	KARCLK#
13	EAUX32	14	KARCS#

Table 31 JS9 Audio Board Connector

Pin	Signal Name	Pin	Signal Name
15	RST#	16	KARDIN#
17	NC	18	KARDOUT#
19	GND	20	NC
21	NC	22	NC
23	RSD	24	TSD3
25	RBCK	26	RWS

Table 32 JS10 SRAM Interface Connector

Pin	Signal Name	Pin	Signal Name
1	LA19	2	LA18
3	LA16	4	LA17
5	LA15	6	LA14
7	LA12	8	LA13
9	LA7	10	LA8
11	LA6	12	LA9
13	LA5	14	LA11
15	LA4	16	LOE#
17	LA3	18	LA10
19	LA2	20	LCS3#
21	LA1	22	LD7
23	LA0	24	LD6
25	GND	26	LD5

Table 33 JS11 EPROM/ROM Emulator Interface Connector

Pin	Signal Name	Pin	Signal Name
1	+5V	2	VCC33
3	LA21	4	LA20
5	LD15	6	LD14
7	LD13	8	LD12
9	LD11	10	LD10
11	LD9	12	LD8
13	LD0	14	WRLL#
15	LD1	16	WRHL#
17	LD2	18	LCS0#
19	LD3	20	LCS2#
21	LD4	22	RST#
23	GND	24	GND

Memory Interface

The evaluation mainboard allows the installation of both an 128-byte EEPROM device, an EPROM or ROM emulator, and 16-, 64- and 128-Mbit SDRAM components. U1 is a 128-byte EEPROM, which is used to store user preferences and system settings.

U4 and U5 can be used to install either an EPROM or a ROM emulator. The socket is capable of supporting up to 1Mbyte of code. Changing R14 or R15 supports either 3.3V or 5.0V devices. Install a 0 ohm resistor at R14 for 5.0V devices or at R15 for 3.3V devices.

All of the Vibratto DVD processors support 16Mbit, 64Mbit and 128Mbit SDRAM components. The evaluation mainboard is designed for 64Mbit or 128Mbit SDRAM parts. The pinout for 64Mbit and 128Mbit SDRAM parts are identical, allowing either type of module to be installed on the board.

Reset

U12 is a Maxim MAX823 microprocessor supervisor. The part generates a 200 ms active-low reset signal after the supply rail has reached the internal threshold voltage. The active-low reset signal then directly connects to the Vibratto. The MAX823 also supports a manual reset feature. Shorting and opening JP1 will initiate a reset signal that is active for 200ms. The manual reset can also be activated through the ROM emulator.

External SRAM/Flash Connectors

Connectors JS10 and JS11 are used for connecting additional memory or I/O devices to the Vibratto, such as the Mod X-Flash module. The signals on the connectors are the RISC processor interface signals, and are the same signals that go the EPROM or ROM emulator socket. Memory spaces corresponding to Banks 0, 2 and 3 are supported.

If the system is to boot from memory connected to these connectors, the memory must be configured to respond to Bank 3 memory space while memory in U4 (EPROM/ROM Emulator) is configured for a different bank or disabled. An example is booting from a Mod X-Flash module. The module would need to be configured for Bank 3 while socket U4 is left empty. If the Mod X-Flash module was being programmed, then the module could be configured for memory Bank 2 while the ROM Emulator in U4 is configured for Bank 3. The Vibratto always boots from the highest address of Bank 3, so the system must be designed accordingly.

Bank 0 is reserved for SRAM only. If SRAM is not used, Bank 0 must be left unconnected.

Audio PLL

U8 is an optional PLL that can be used to generate the master audio clock for the DAC, ADC and the Vibratto. The parts can be programmed to generate a variety of frequencies. The following frequencies used by the audio PLL are listed in Table 34.

Table 34 U8 Audio PLL Sampling Frequencies

Sampling Rate (kHz)	256Fs (MHz)	384Fs (MHz)	192Fs (MHz)
32.0	8.192	12.288	N/A
44.1	11.2896	16.9344	N/A
48.0	12.288	18.432	N/A
64.0	16.384	24.576	N/A
88.2	22.5792	33.6688	N/A
96.0	24.576	36.864	N/A
192.0	N/A	N/A	36.864

Audio Input

Analog audio is input to the Vibratto evaluation mainboard through JS7. The maximum input level is 1Vrms (0db). The analog audio is converted into digital form by a PCM1800 ADC from Texas Instruments/Burr-Brown. The PCM1800 is a 20-bit, 2-channel device capable of sampling rates up to 48KHz. Both master and slave modes are supported by the PCM1800, but on the evaluation board, the PCM1800 has been configured for master mode operation. Master mode was selected so that the audio receive port on the Vibratto could be run at a different sample rate from the audio transmit port. Additional ADCs can be tested using connector JS9.

Video, VFD and S/PDIF

The Vibratto evaluation mainboard has been configured to use the internal video encoder. The analog video and the horizontal and vertical sync signals are output on JS3. A back-end board having 75ohm termination, video filtering, ESD protection, and the appropriate connectors are needed to correctly interface to a TV. At this time, only the VDAC output has the termination and filtering implemented on the same circuit board as the Vibratto. This was done as an example of how a simple filtering circuit could be designed.

JS5 is used to connect a front panel to the Vibratto evaluation mainboard. Infrared input is supported along with any Vacuum Fluorescent Display (VFD) controller supporting a 3-wire interface. The infrared input should be a demodulated TTL-level signal. Power (+5V) is also provided on the connector for the VFD controller, but the filament voltage for the display must be supplied externally.

The S/PDIF output from the Vibratto is a TTL-level digital signal. Connector JS6 is used to output the S/PDIF signal. This signal is must be sent to a line driver circuit before being sent to an external decoder.

About The DVD-Audio Daughterboard

The DVD-Audio daughterboard is designed to demonstrate the 6-channel DVD-audio features and karaoke features of the Vibratto DVD processor. The daughterboard inputs 6-channel digital audio from an ESS DVD decoder board and converts it into 6 channels of Dolby Digital-compliant analog audio. Included on the demo board is a Yamaha YSS903 for karaoke processing, S/PDIF output circuit, and an anti-aliasing filter for NTSC or PAL video.

Daughterboard Features

The DVD-Audio daughterboard supports the following features:

- Dolby Digital compliant
- 6 channels of 24-bit audio at a maximum sampling rate of 96 kHz
- 2 channels of 24-bit audio at a maximum sampling rate of 192 kHz
- Supports AKM AK4356 or Wolfson WM8736 audio DACs
- Karaoke processing with Yamaha YSS903
- CD-DA audio bypass option
- Coax and optical S/PDIF output
- NTSC/PAL video output
- RF modulator output option
- Composite video output
- S-Video output
- Component (YUV) video output
- RGB video output

Functional Description

The DVD-Audio daughterboard is designed to meet all the requirements of the Dolby Digital simplified configuration. Audio is sent from the DVD decoder main board to the daughterboard through JS2.

From JS2, the audio is sent in digital form to either an AKM AK4356 or a Wolfson WM8736 audio DAC for digital-to-analog conversion. The analog audio from the audio DAC is sent through several filters for anti-aliasing and bass redirection, as required by the Dolby Digital specifications.

Figure 42 identifies the available high-pass and low-pass filter configurations. Output at the RCA connector is 2.0 V_{rms}.

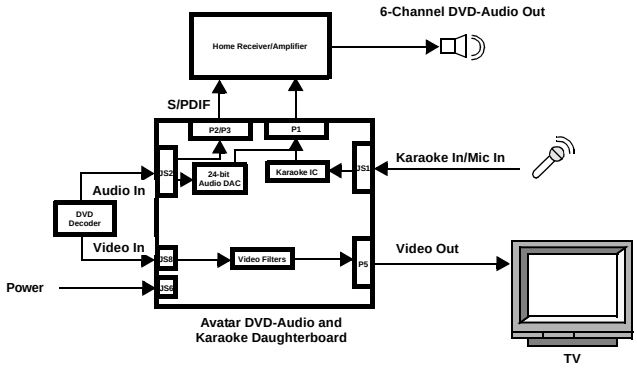


Figure 42 High-Pass and Low-Pass Filter Configurations

Included on the daughterboard is a Yamaha YSS903 karaoke processor. Microphone input is through JS1. The output of the YSS903 is summed with the front left and front right channels from the audio DAC. Programming and control of the YSS903 is done from the DVD decoder mainboard.

To control the YSS903 karaoke device on the daughterboard, U9, U10 and U11 were added to the board as additional logic. U9 is used as a decoder on the RISC bus. The output of U9 is used to clock data into latch U11, which drives the signals for the YSS903, and an onboard PLL. U10 is a tri-state buffer that drives data from the YSS903 on to the RISC bus. Two of the decoder outputs of U9 are routed to the JS1 DVD drive expansion connector for use by external devices.

Depending on the number of I/Os and type of logic used in the design, a decoder may not be needed. This design used memory Bank 1 for I/O, but Bank 2 is also usable for the same purpose. Banks 0 and 3 are not recommended for this purpose because of memory addressing issues.

Figure 43 is the daughterboard block diagram.

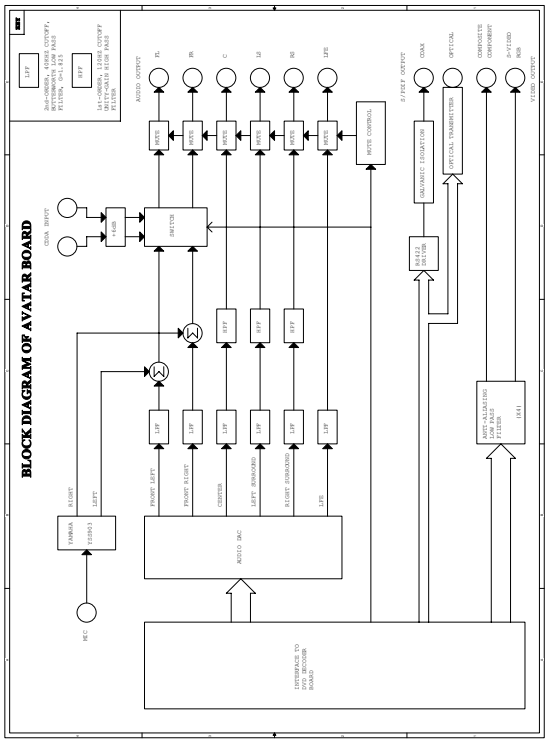


Figure 43 Daughterboard Block Diagram

Figure 44 is a diagram showing all the connections on the Avatar board, including pinouts for connectors P1 and P5.

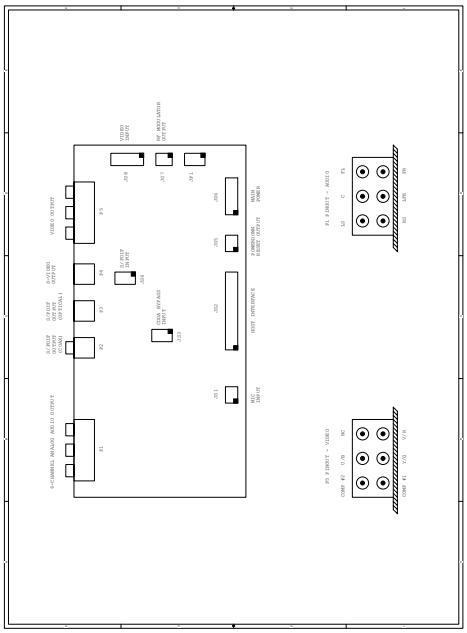


Figure 44 Daughterboard Connectors

For DVD drives that output CD-DA audio only in analog form, the daughterboard includes an option for CD-DA bypass. The CDDA audio is fed into JS3 where it is amplified by +6-dB before being passed through a selector/switch circuit. The +6 dB gain can be changed based on the output of the specific drive. The expected amplitude of the CDDA audio is $1V_{rms}$.

S/PDIF is input to the daughterboard through JS4 as a TTL-level signal. The TTL-level signal is sent to an RS-422 driver and an optical transmitter. The output of the RS-422 driver is galvanically isolated in accordance with IEC958 specifications (unbalanced line), and then sent to connector P2 for output. The output of P2 is 500 mV_{p-p}, when measured across a 75-ohm resistor connected at the output.

The video signal from the ESS DVD decoder board is input on JS8. This signal passes through a passive anti-aliasing low-pass filter before being output on P4 and P5. The video signals are arranged to provide representative combinations of video output options, including composite, S-video, component, and RGB. The exact output of the various connectors will vary, depending on the version of the DVD Decoder mainboard being used. An option for and RF modulator output is included on the daughterboard. Refer to the description for JP1 for more details.

Jumpers

Jumper JP1 is used to select if the second composite video output is to be directed to an RCA connector or an RF modulator module. Connecting pins 1 and 2 will select the RCA connector while connecting pins 2 and 3 will select the RF modulator. Table 35 summarizes the jumper settings for JP1.

Table 35 JP1 Jumper Settings

JP1—Position	Signal Name
1 and 2	RCA Connector
2 and 3	RF Modulator

Connector Pin Assignments

Table 36 through Table 42 list the connectors on the daughterboard and the corresponding signal names.

Table 36 JS1 MIC Input

Pin	Signal Name	Pin	Signal Name
1	MIC	2	GND

Table 37 JS2 DVD Decoder Interface

Pin	Signal Name	Pin	Signal Name
1	AUDCLK	14	KARCS#
2	GND	15	EXTRST#
3	TBCK	16	KARDIN
4	TSDA	17	PWRDN
5	TWS	18	KARDOUT
6	TSDB	19	GND
7	GND	20	CDFIX
8	TSDC	21	SMUTE
9	CNTLA	22	NC
10	GND	23	NC
11	CNTLB	24	NC
12	KARCLK#	25	NC
13	CNTLC	26	NC

Table 38 JS4 S/PDIF Input Interface

Pin	Signal Name	Pin	Signal Name
1	LEFT	3	GND
2	GND	4	RIGHT

Table 39 JS5 Reset/Powerdown

Pin	Signal Name	Pin	Signal Name
1	RESET/ PWRDN	2	GND

Table 40 JS6 Daughterboard Power Connector

Pin	Signal Name	Pin	Signal Name
1	VCC (+5V)	4	+12V
2	GND	5	–12V
3	GND	6	NC

Table 41 JS7 Coax Modulator Output

Pin	Signal Name	Pin	Signal Name
1	Composite	2	GND

Table 42 JS8 Video Input

Pin	Signal Name	Pin	Signal Name
1	CVBS1	4	CHROMA
2	GND	5	NC
3	LUMA	6	CVBS2

APPENDIX A: MAINBOARD REFERENCE DESIGN SCHEMATICS

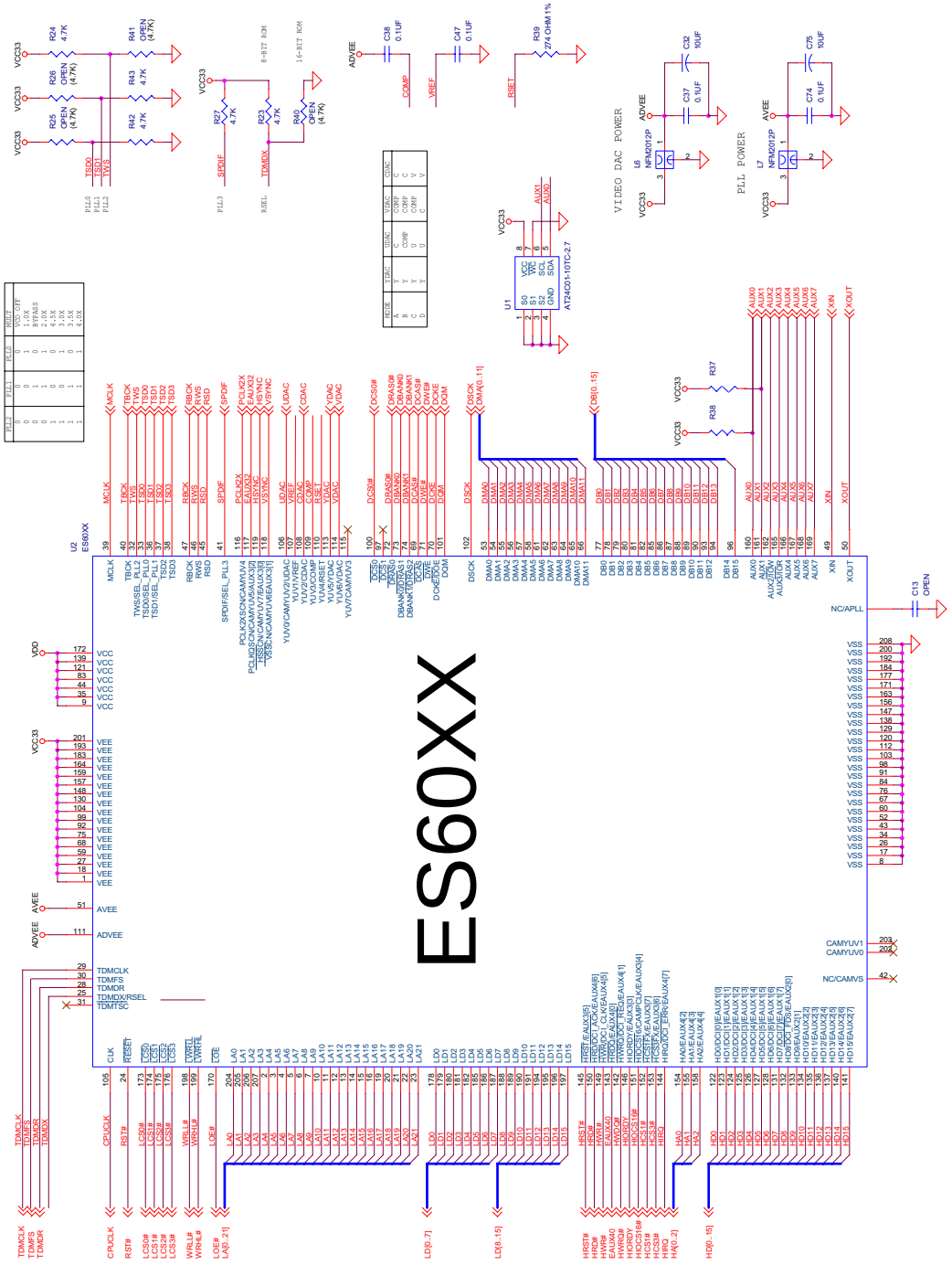


Figure 45 ES60x8 Device Interface

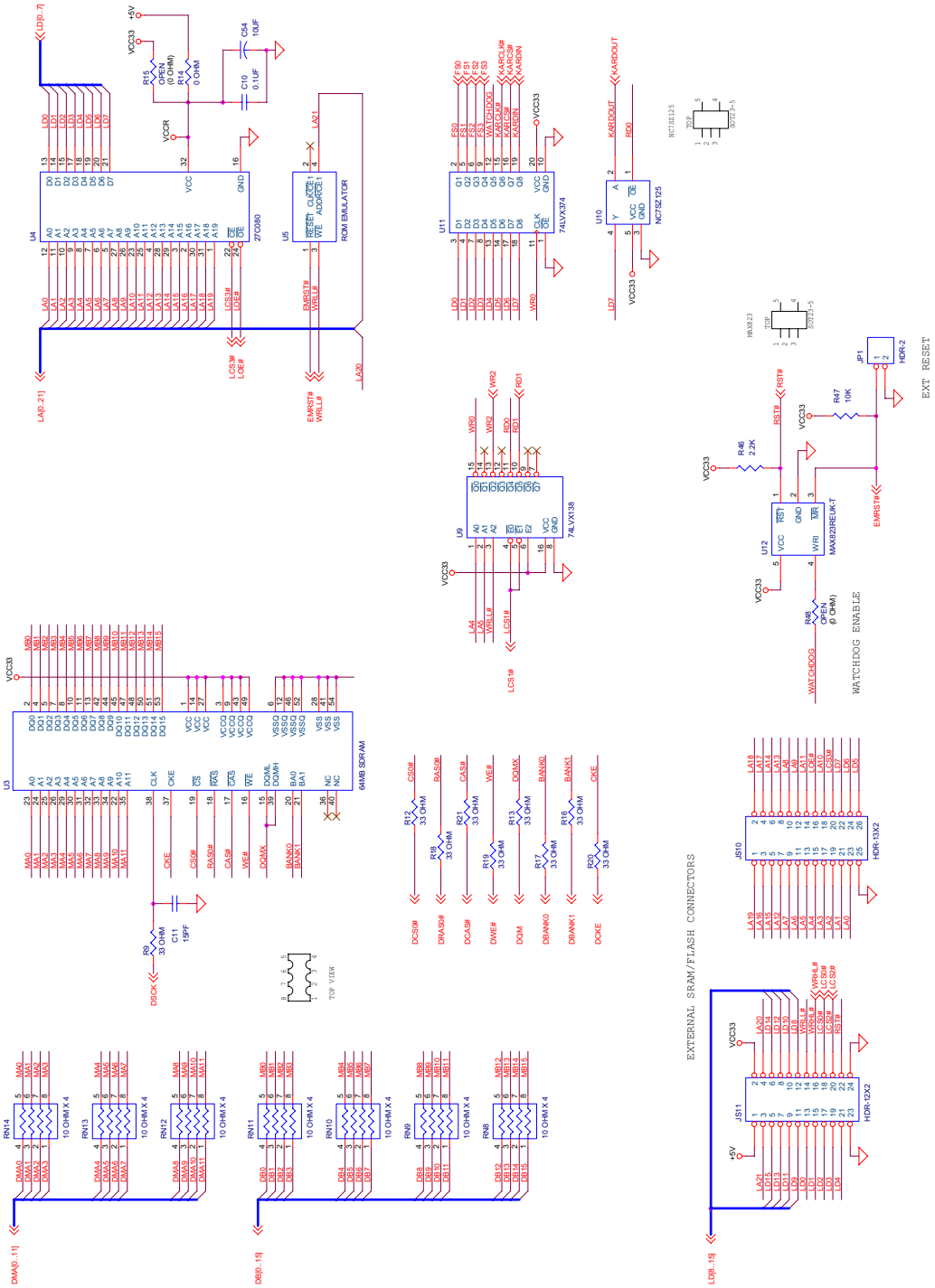


Figure 46 Memory Interface

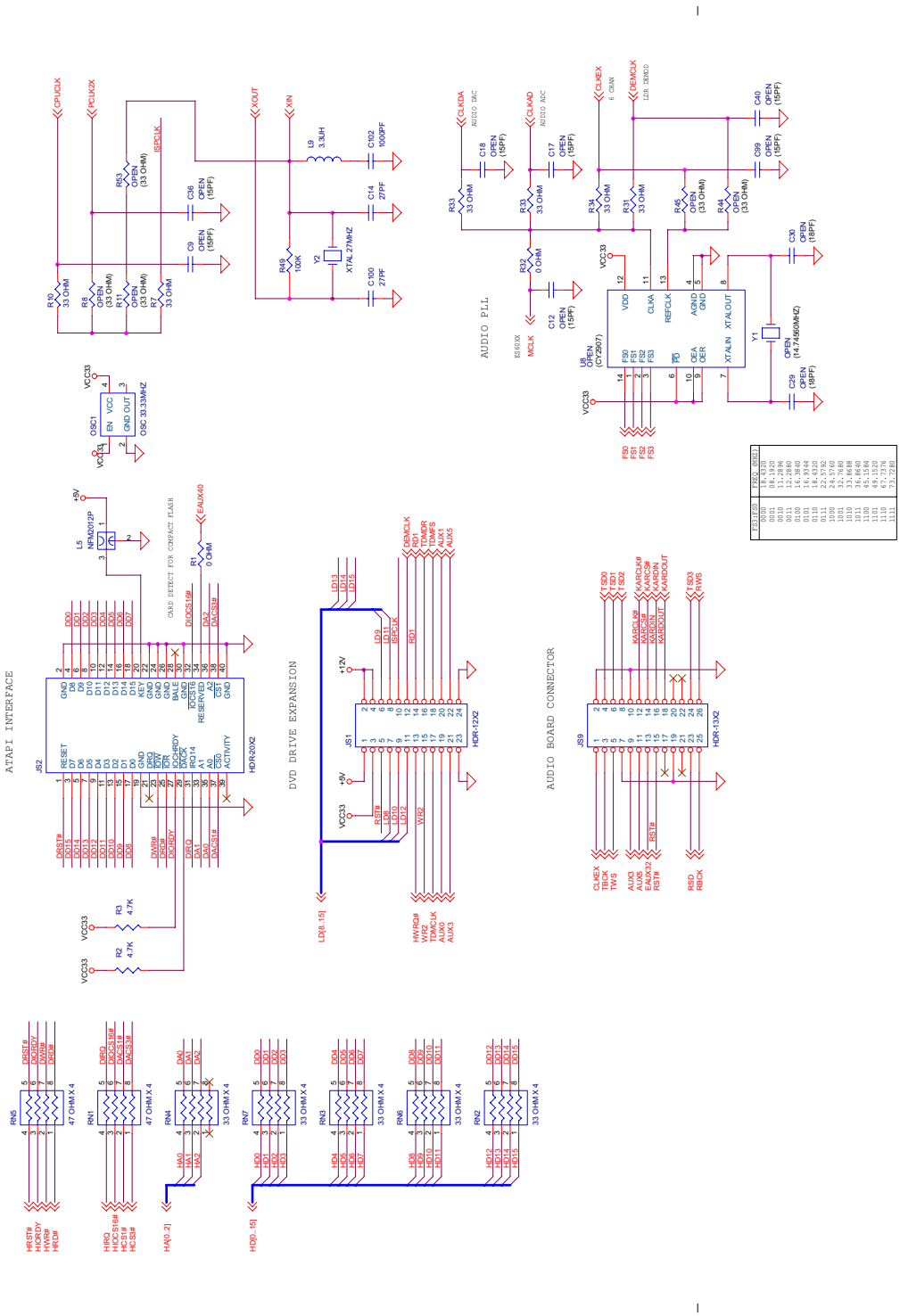


Figure 47 ATAPI Interface

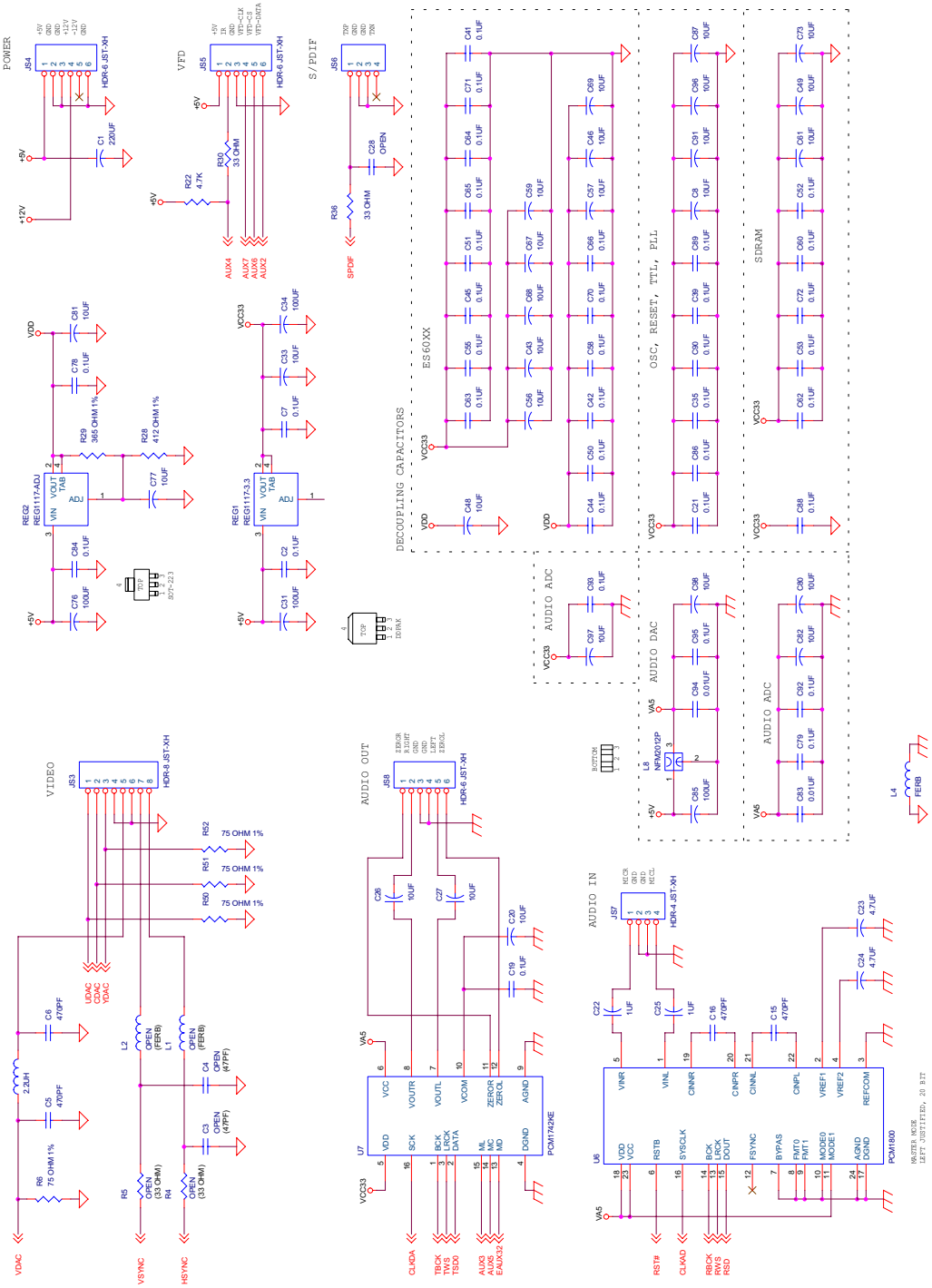


Figure 48 Video and Audio DACs

APPENDIX B: MAINBOARD BILL OF MATERIALS

Table 43 Bill of Materials

Item	Qty	Location	Description
Capacitors, SMD			
1	4	C5, C6, C15, C16	CAP, CER, SMT, 0805, 470pF, 5%, 50V, NPO
2	2	C83, C94	CAP, CER, SMT, 0805, 0.01µF, 10%, 25V, X7R
3	40	C2, C7, C10, C19, C21, C35, C37, C38, C39, C41, C42, C44, C45, C47, C50, C51, C52, C53, C55, C58, C60, C62, C63, C64, C65, C66, C70, C71, C72, C74, C78, C79, C84, C86, C88, C89, C90, C92, C93, C95	CAP, CER, SMT, 0805, 0.1µF, 10%, 25V, X7R
4	2	C22, C25	CAP, TANT, SMT, CASE A, 1µF, 20%, 25V
5	2	C23, C24	CAP, TANT, SMT, CASE A, 4.7µF, 20%, 16V
6	29	C8, C20, C26, C27, C32, C33, C43, C46, C48, C49, C54, C56, C57, C59, C61, C67, C68, C69, C73, C75, C77, C80, C81, C82, C87, C91, C96, C97, C98	CAP, TANT, SMT, CASE A, 10µF, 20%, 16V
7	4	C31, C34, C76, C85	CAP, TANT, SMT, CASE C, 100µF, 20%, 10V
Capacitors, Through Hole			
8	1	C1	CAP, ALUM, RADIAL, 220µF, 20%, 25V, 2.5mm LS
Resistors, SMD, 5%			
9	3	R1, R15, R32	RES, SMT, 0805, 0 OHM, 5%, 1/10W
10	1	R9	RES, SMT, 0805, 10 OHM, 5%, 1/10W
11	18	R7, R8, R10, R11, R12, R13, R16, R17, R18, R19, R20, R21, R30, R31, R33, R34, R35, R36	RES, SMT, 0805, 33 OHM, 5%, 1/10W
12	2	R37, R38	RES, SMT, 0805, 1K, 5%, 1/10W
13	1	R46	RES, SMT, 0805, 2.2K, 5%, 1/10W
14	9	R2, R3, R22, R23, R24, R27,R40, R42, R43	RES, SMT, 0805, 4.7K, 5%, 1/10W
15	1	R47	RES, SMT, 0805, 10K OHM, 5%, 1/10W
Resistors, SMD, 1%			
16	1	R6	RES, SMT, 0805, 75 OHM, 1%, 1/10W
17	1	R39	RES, SMT, 0805, 274 OHM, 1%, 1/10W
18	2	R28, R29	RES, SMT, 0805, 412 OHM, 1%, 1/10W
Resistor Arrays, SMD, 5%			
19	7	RN8, RN9, RN10, RN11, RN12, RN13, RN14	RES, ARRAY, 10 OHM, 5%, 1/6W, 4 RES, ISOLATED BOURNS CAY16-100J4
20	5	RN2, RN3, RN4, RN6, RN7	RES, ARRAY, 33 OHM, 5%, 1/6W, 4 RES, ISOLATED BOURNS CAY16-330J4
21	2	RN1, RN5	RES, ARRAY, 47 OHM, 5%, 1/6W, 4 RES, ISOLATED BOURNS CAY16-330J4
Ferrites, Inductors and EMI Filters			
22	1	L4	FERRITE BEAD, 1210
23	1	L3	INDUCTOR, 2.2µH, 1210
24	4	L5, L6, L7, L8	EMI FILTER, NFM2012P13C105F, MURATA, 0805
Voltage Regulators			
25	1	REG2	REG, REG1117-ADJ, BURR-BROWN, SOT-223
26	1	REG1	REG, REG1117-3.3, BURR-BROWN, DDPAK

Table 43 Bill of Materials (Continued)

Item	Qty	Location	Description
Headers & Connectors			
27	1	JP1	HEADER, 2X1, 0.1" CENTERS
28	2	JS7,JS6	HEADER, 4X1, 0.1" CENTERS, JST-XH
29	3	JS4,JS5,JS8	HEADER, 6X1, 0.1" CENTERS, JST-XH
30	1	JS3	HEADER, 8X1, 0.1" CENTERS, JST-XH
31	2	JS11,JS1	HEADER, 12X2, 0.1" CENTERS
32	2	JS10,JS9	HEADER, 13X2, 0.1" CENTERS
33	1	JS2	HEADER, 20X2, 0.1" CENTERS
Sockets			
34	1	U5	ROM EMULATOR
35	1	U4	SOCKET, DIP-32, 0.6"
Oscillators & Crystals			
36	1	OSC1	OSC, 27MHZ, SMT, EPSON SG-636PCE 27.000M2
37	1	Y1	CRYSTAL, 14.74560MHZ, 18PF, HCM-49
ICs			
38	1	U2	IC, ES6038, PQFP-208
39	1	U3	IC, SDRAM, 64Mb, 1Mx16x4, 133MHz, 7.5NS, 54 TSOP
40	1	U1	IC, EEPROM, AT24C01-10TC-2.7, SO-8, ATMEL
41	1	U12	IC, RESET, MAX823REUK-T, SOT23-5, MAXIM
42	1	U11	IC, 74LVX374, TSSOP-20, FAIRCHILD
43	1	U9	IC, 74LVX138, TSSOP-16, FAIRCHILD
44	1	U10	IC, NC7SZ125, SOT23-5, FAIRCHILD
45	1	U8	IC, PLL, CY2907, CYPRESS, SO-14
46	1	U7	IC, AUDIO DAC, PCM1742KE, SSOP-16, BURR-BROWN
47	1	U6	IC, AUDIO ADC, PCM1800, SSOP-24, BURR-BROWN

APPENDIX C: MAINBOARD GERBER FILES

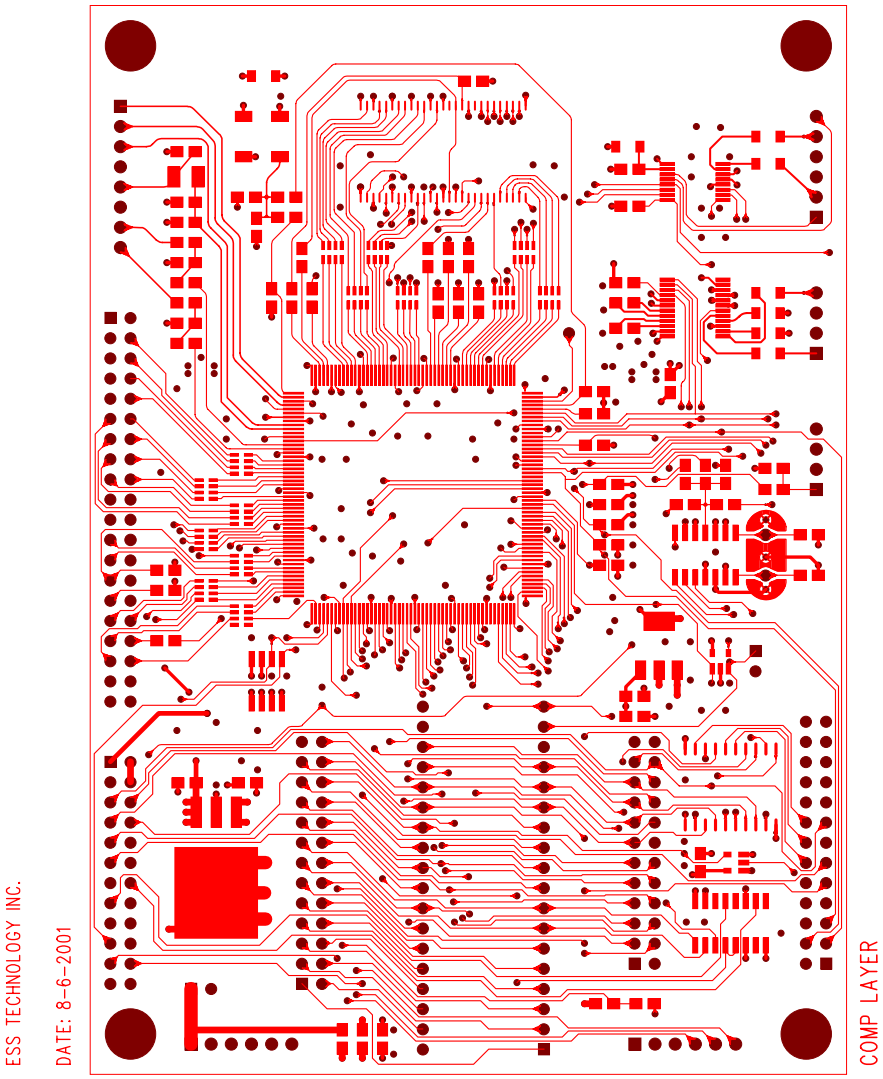


Figure 49 Component Layer

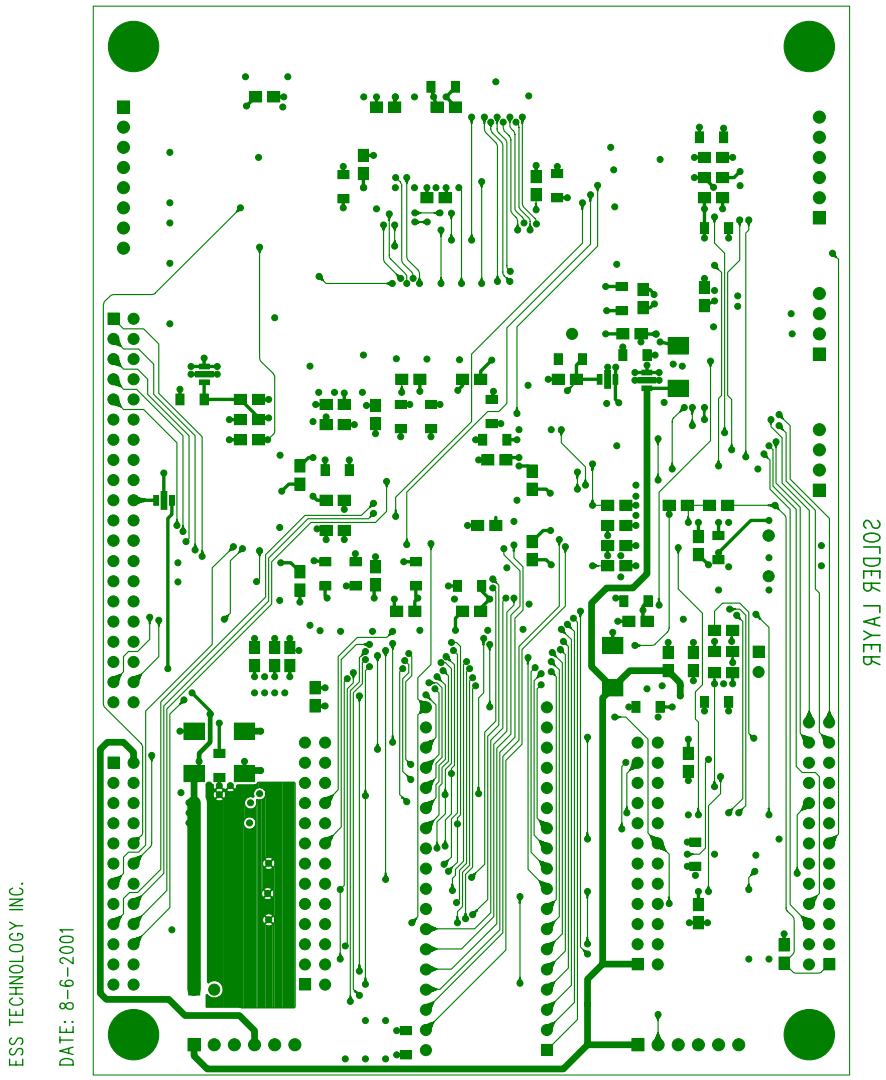


Figure 50 Solder Layer

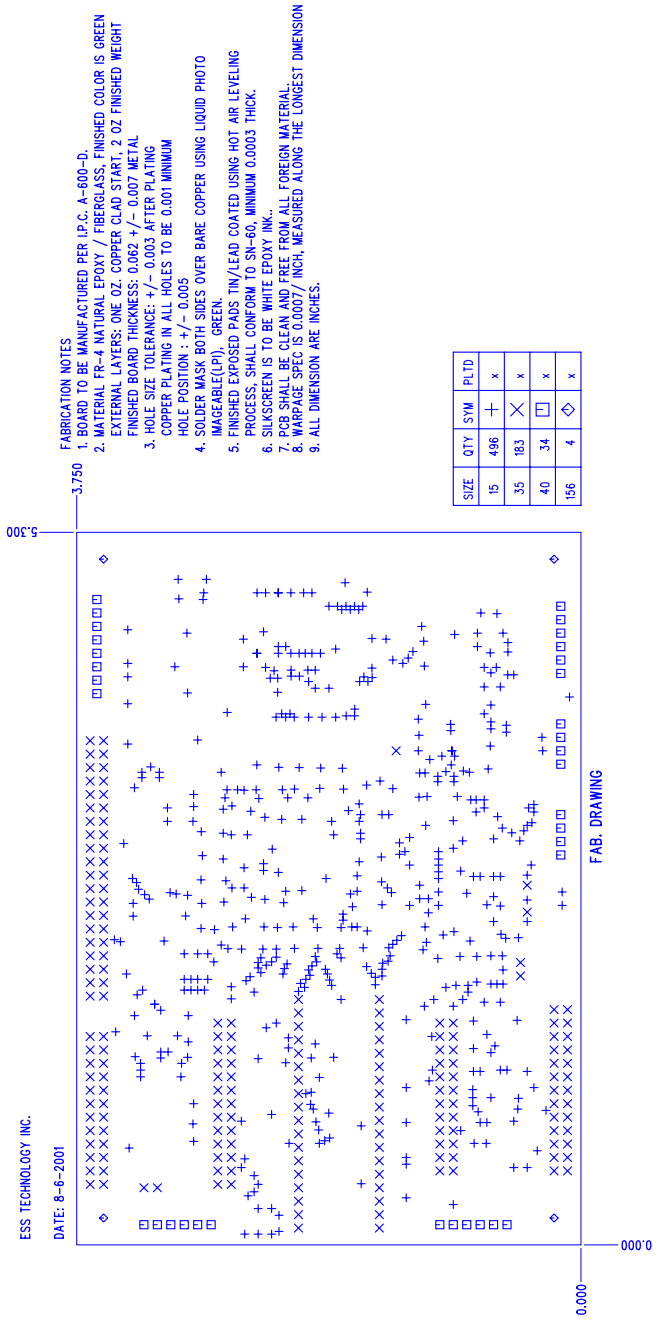


Figure 51 Drill Template

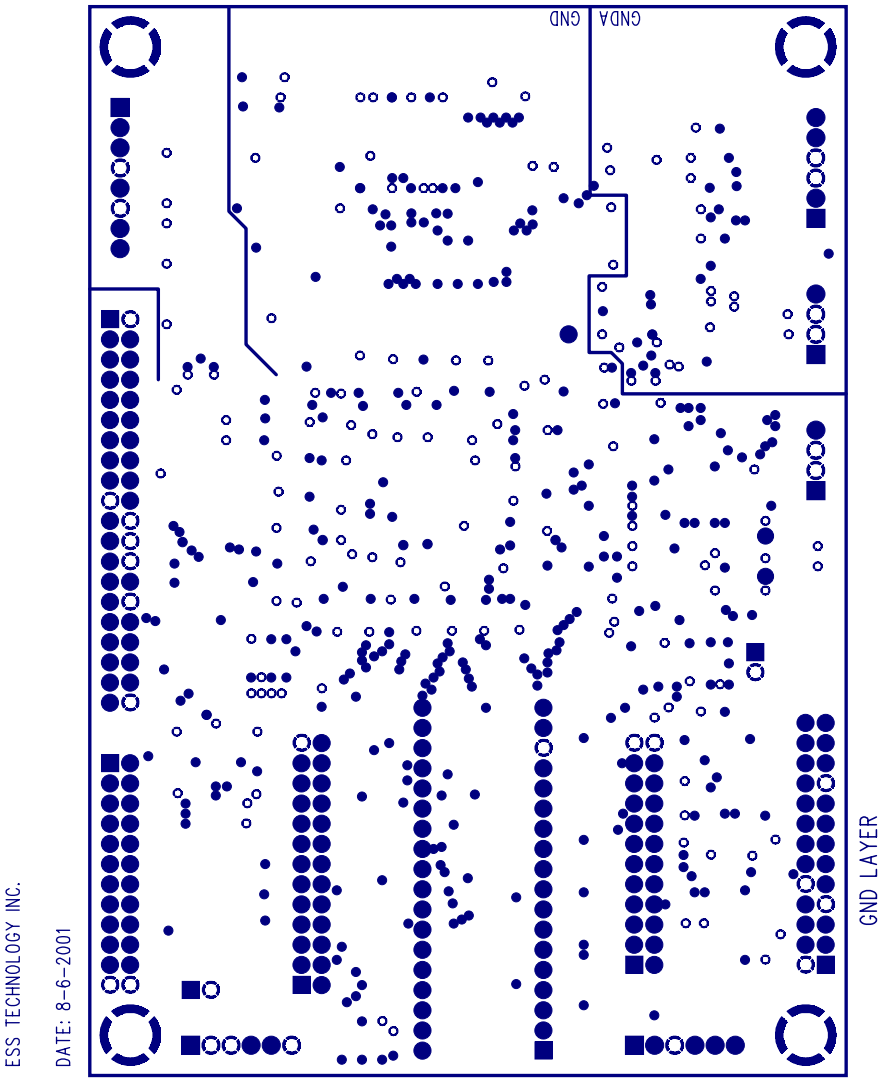


Figure 52 Ground Plane

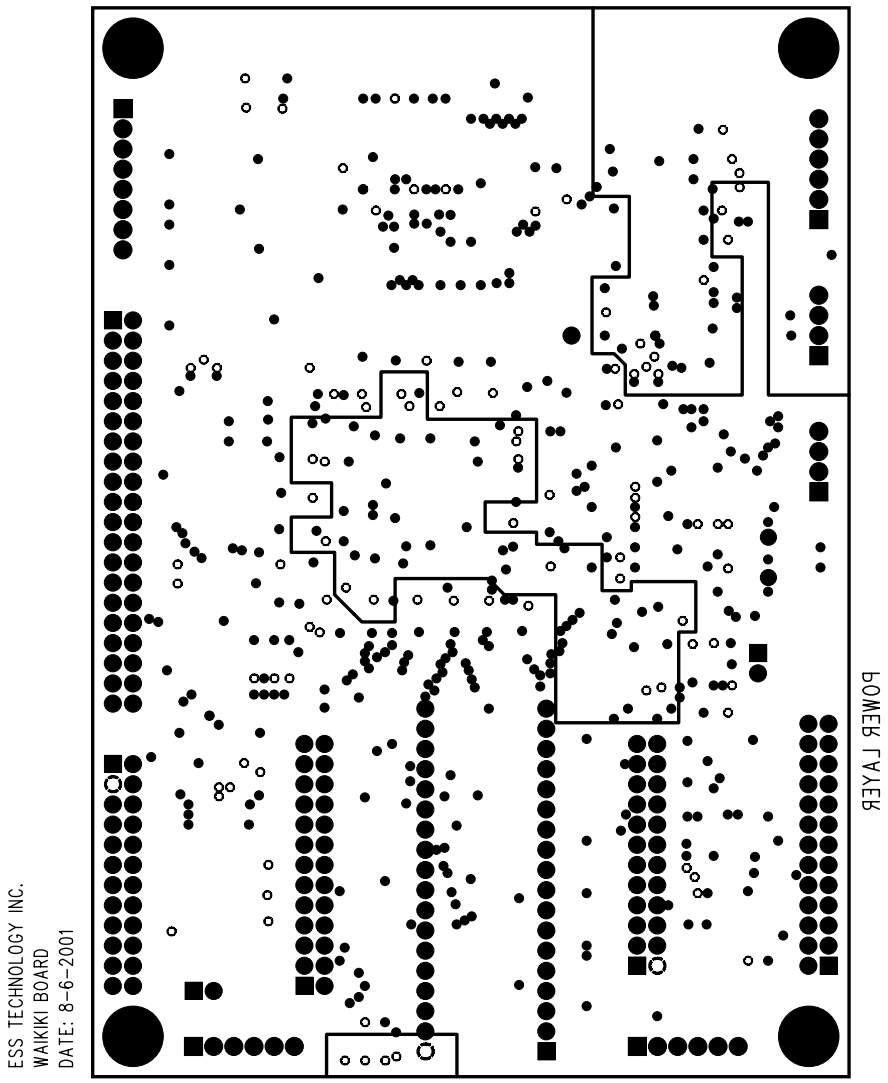


Figure 53 Power Layer

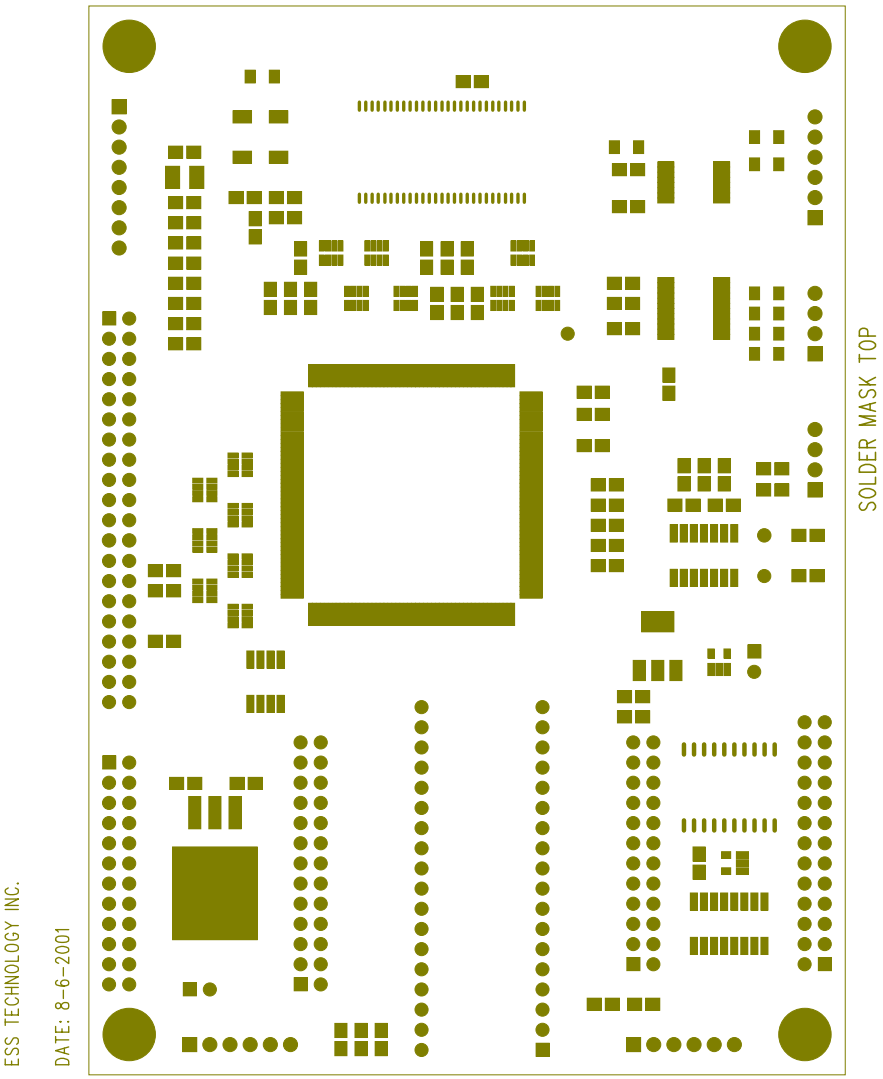


Figure 54 Solder Mask Top Layer

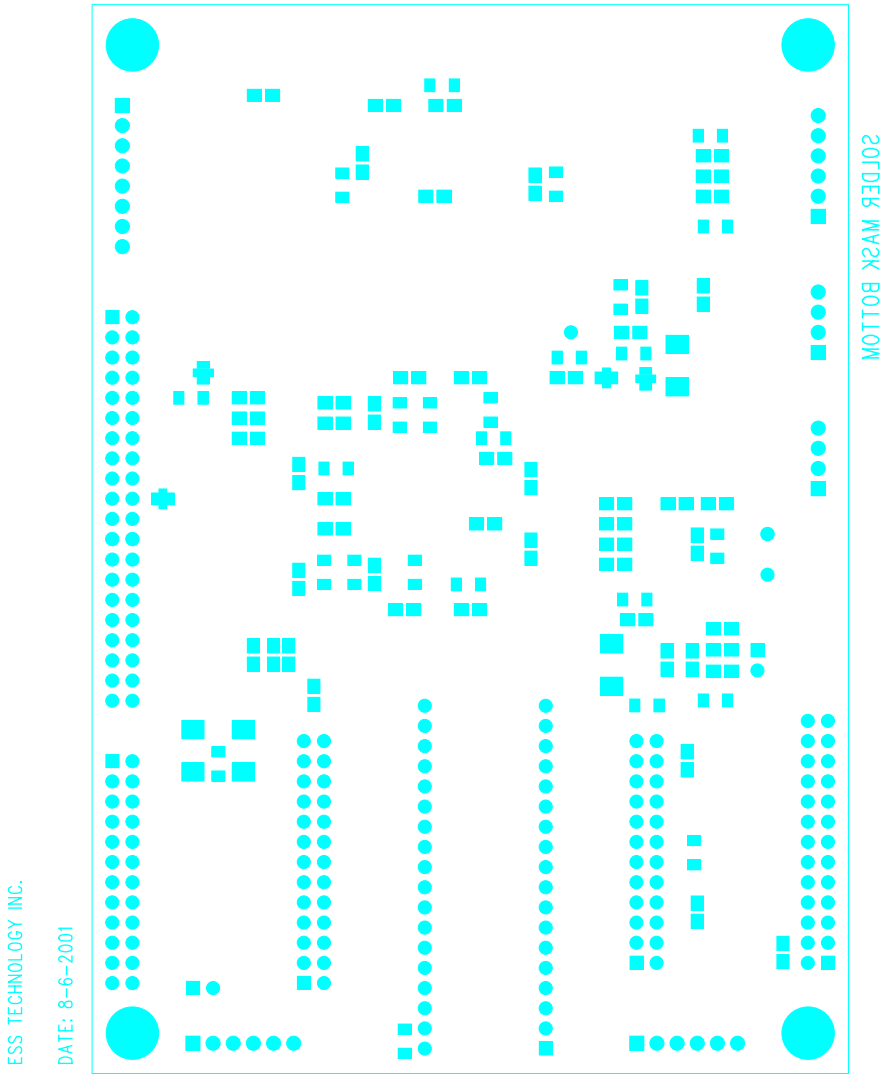


Figure 55 Solder Mask Bottom Layer

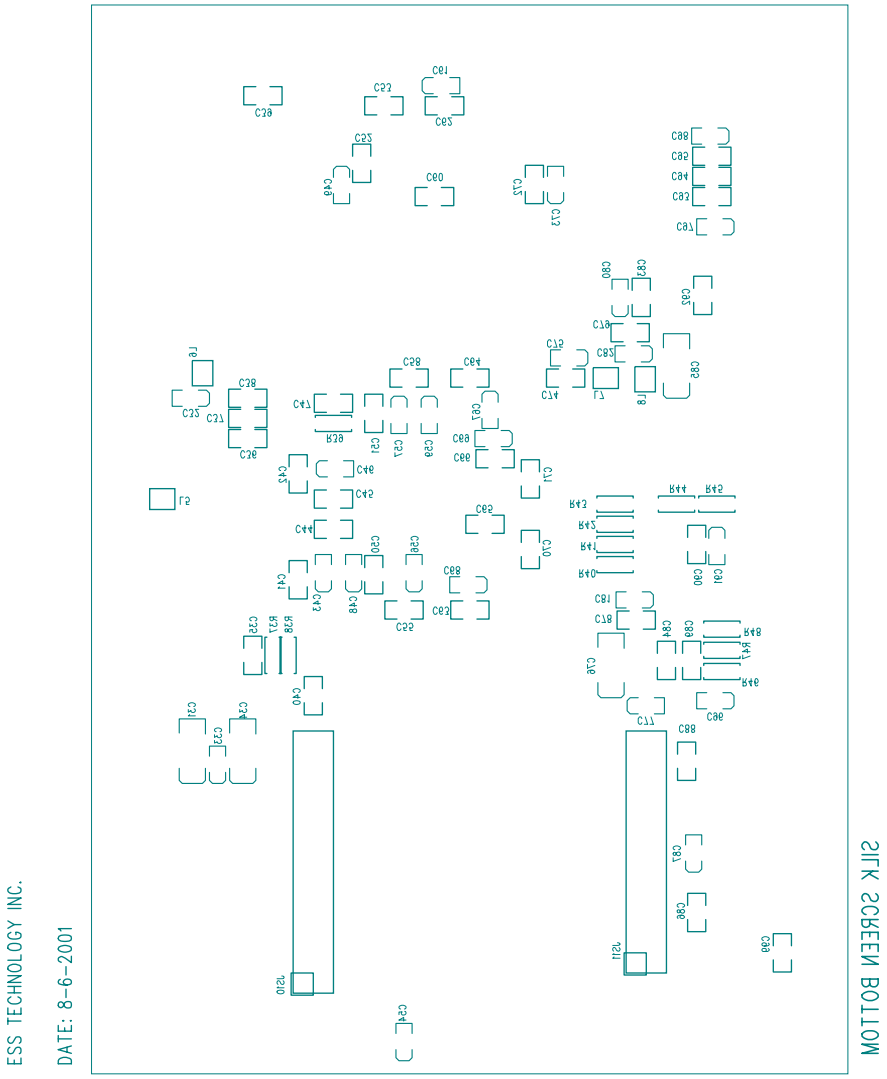


Figure 56 Silkscreen Bottom Layer

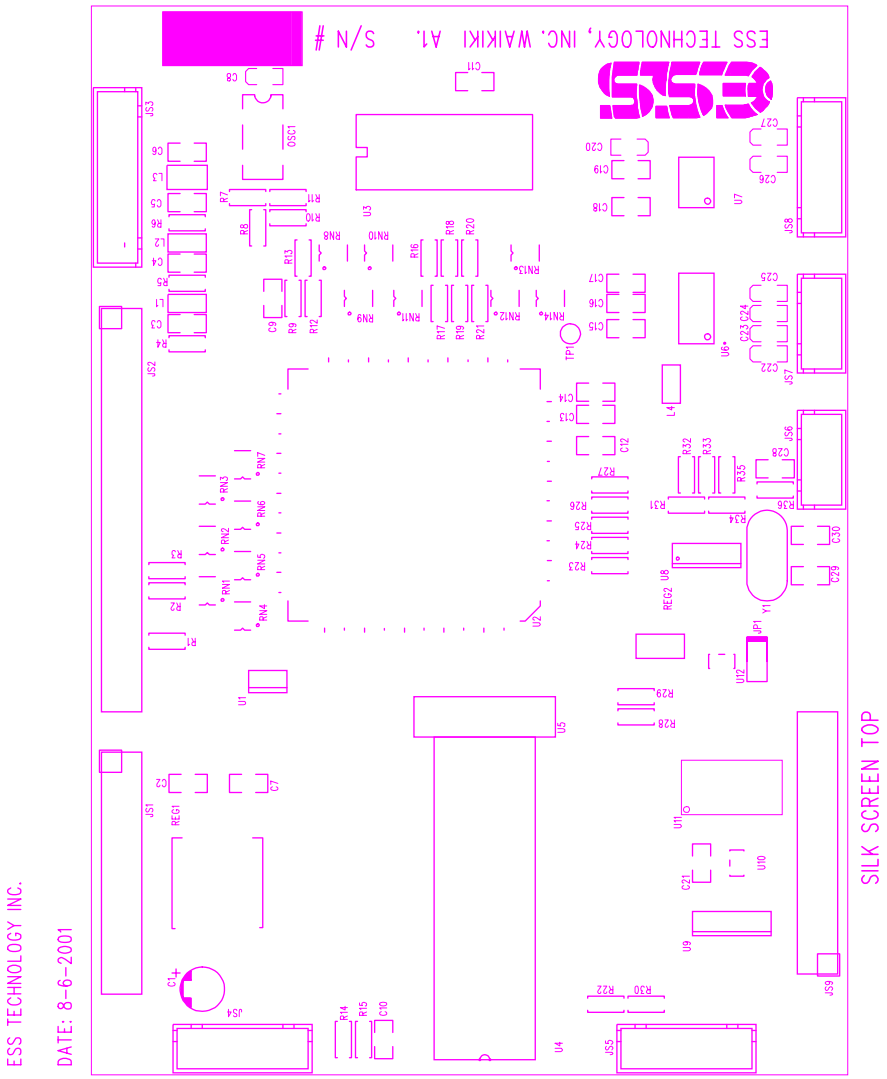


Figure 57 Silkscreen Top Layer

APPENDIX D: DVD-AUDIO DAUGHTERBOARD SCHEMATICS

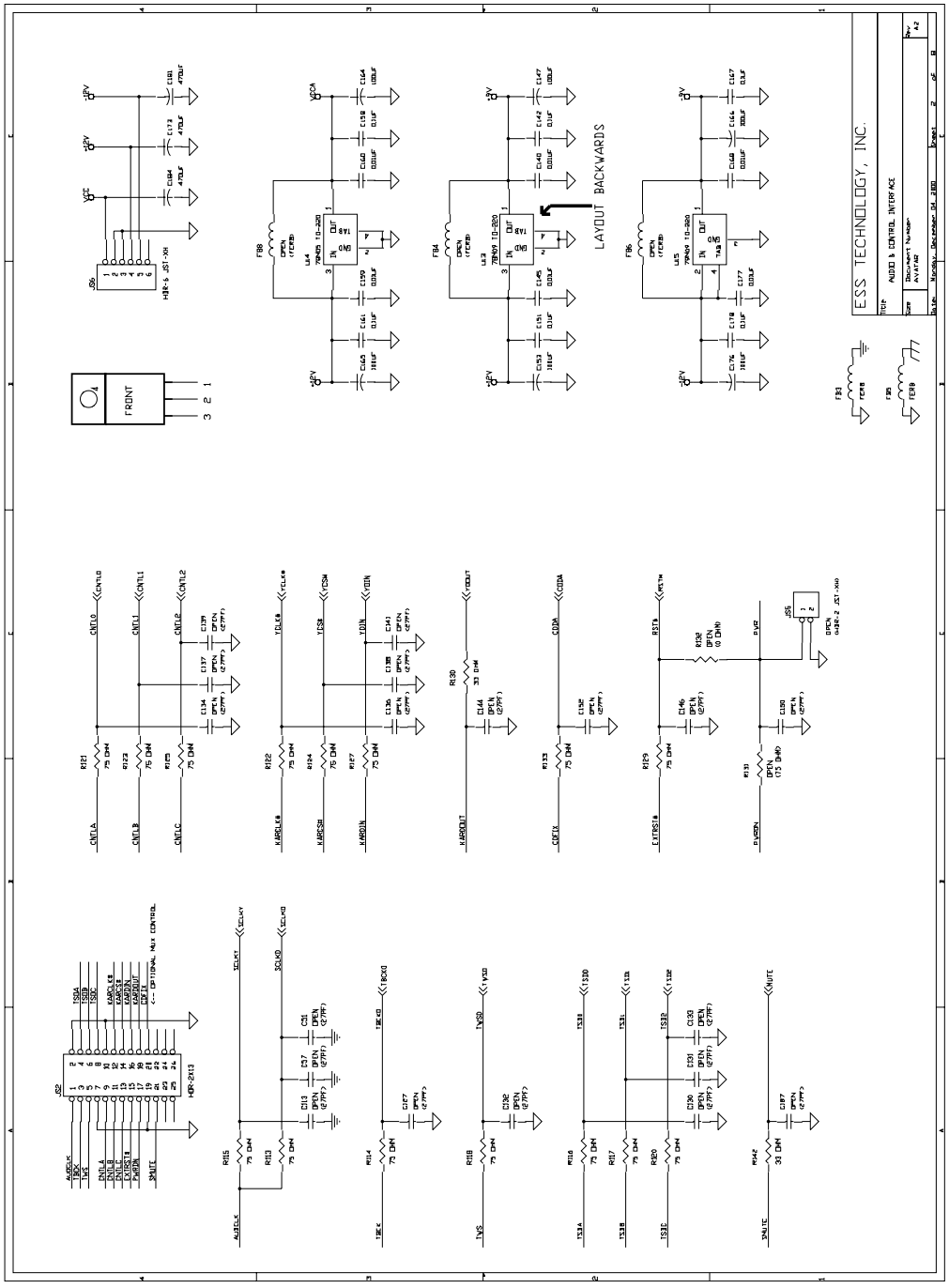


Figure 58 Audio and Control Interface

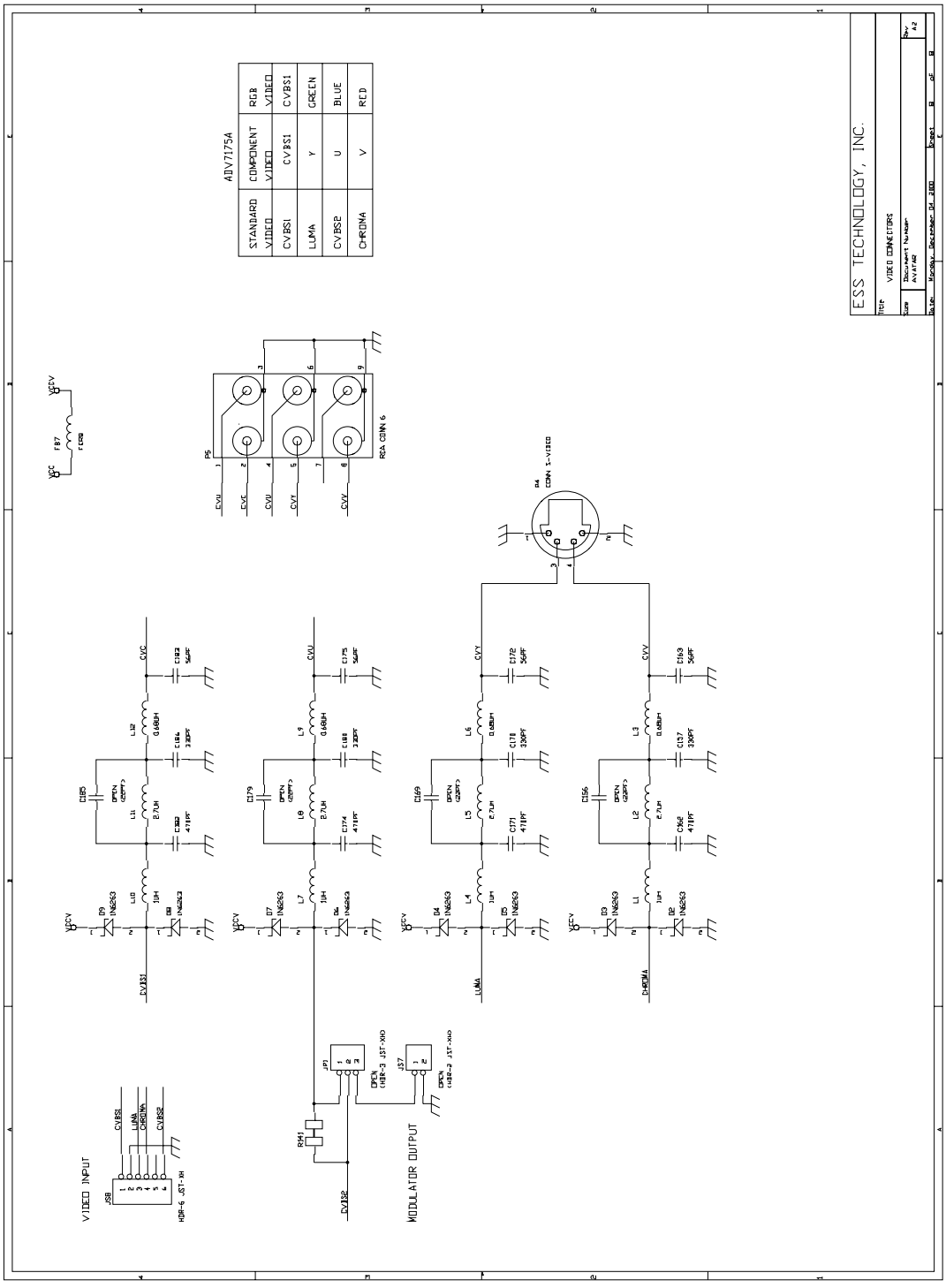


Figure 59 Video Connectors

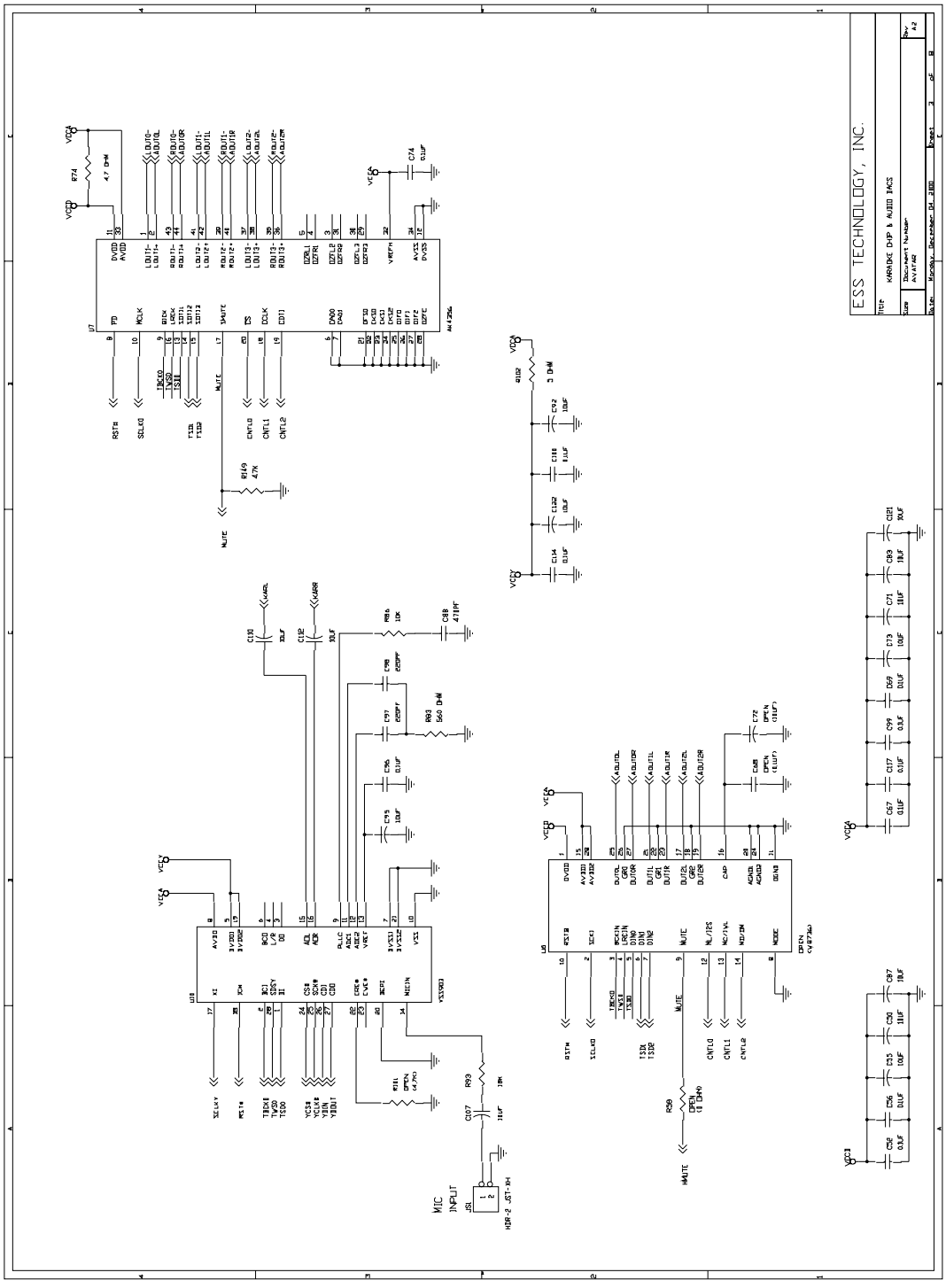


Figure 60 Karaoke and Audio DACs

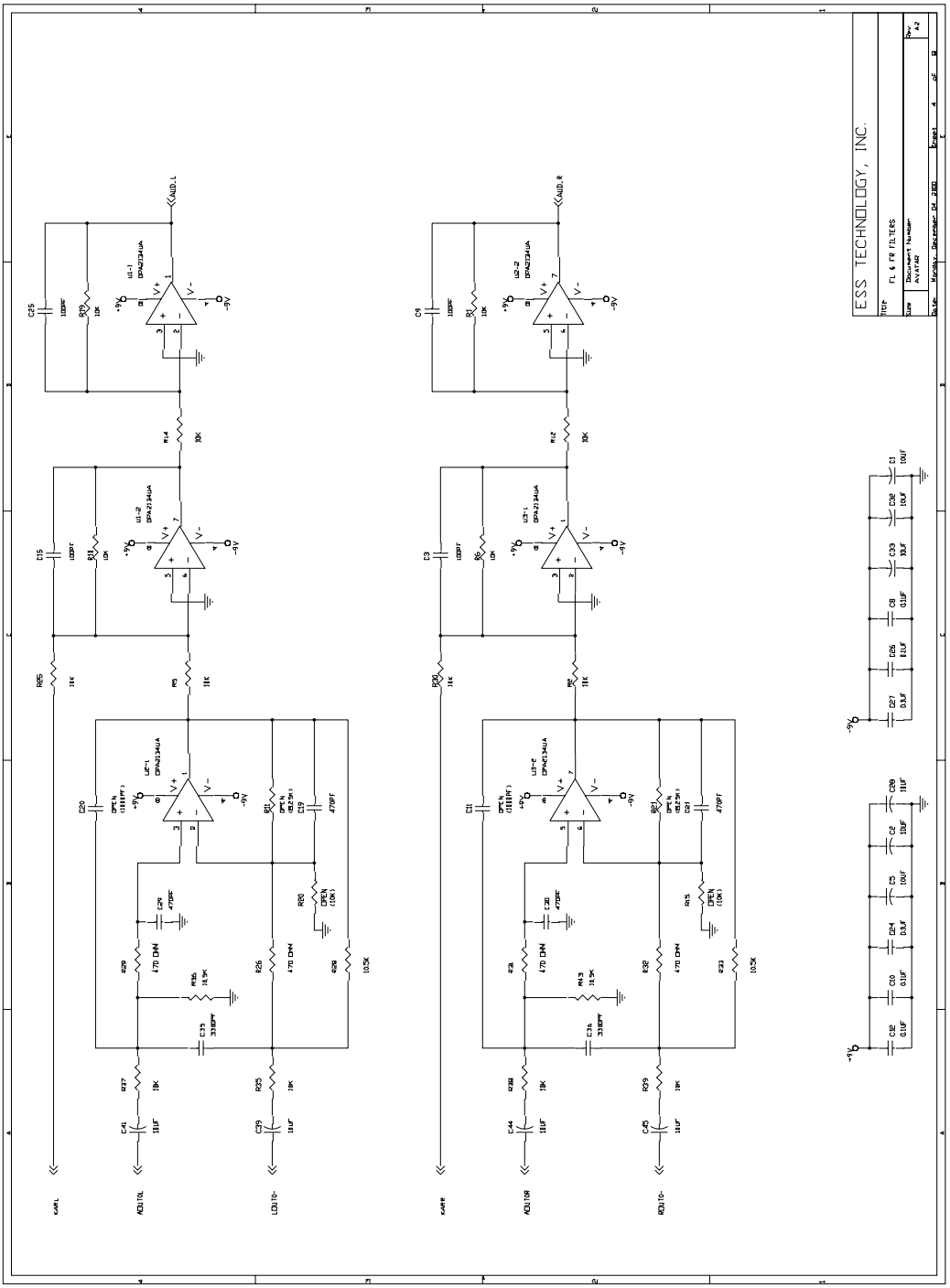


Figure 61 FL and FR Filters

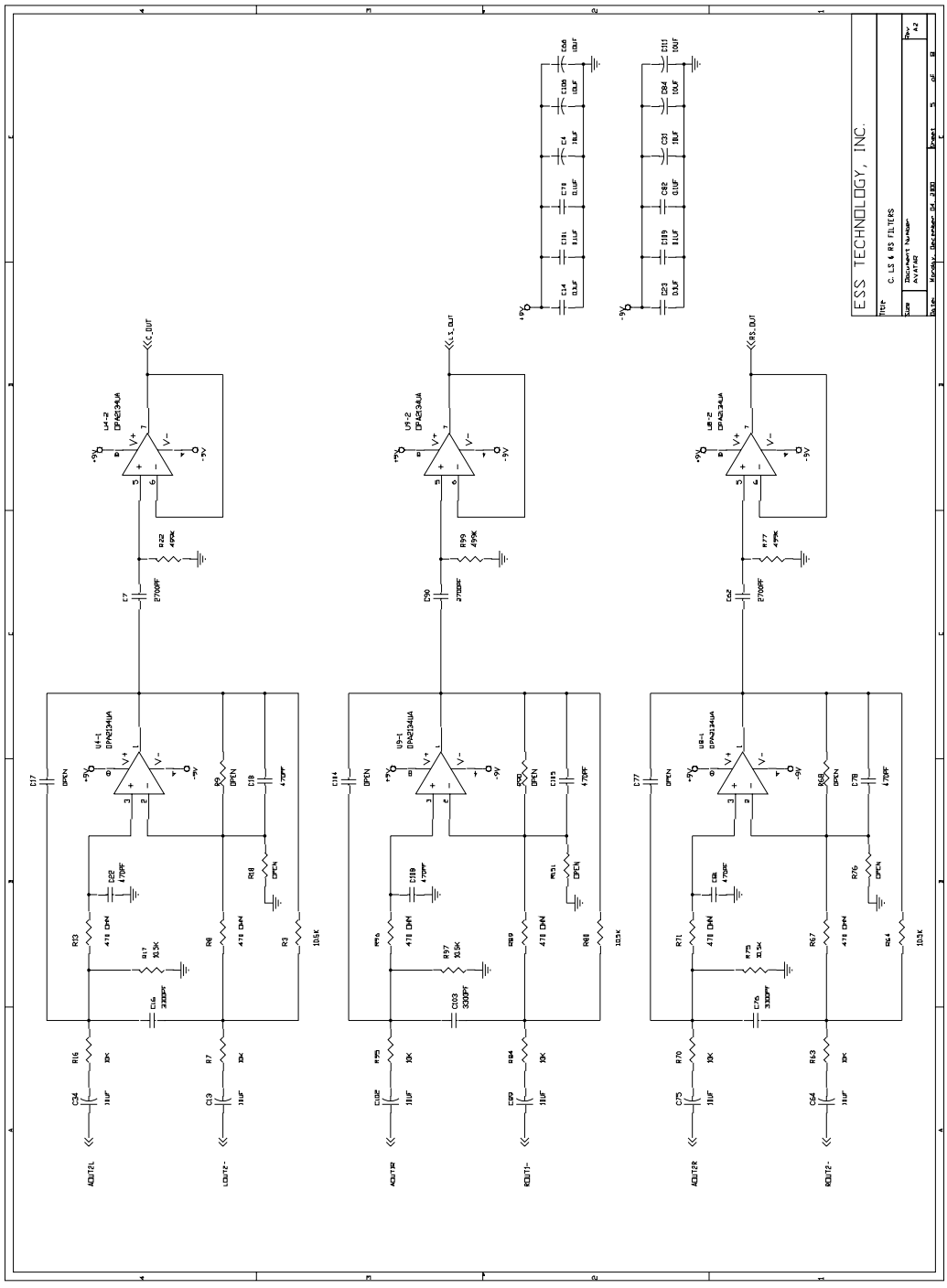


Figure 62 C, LS and RS Filters

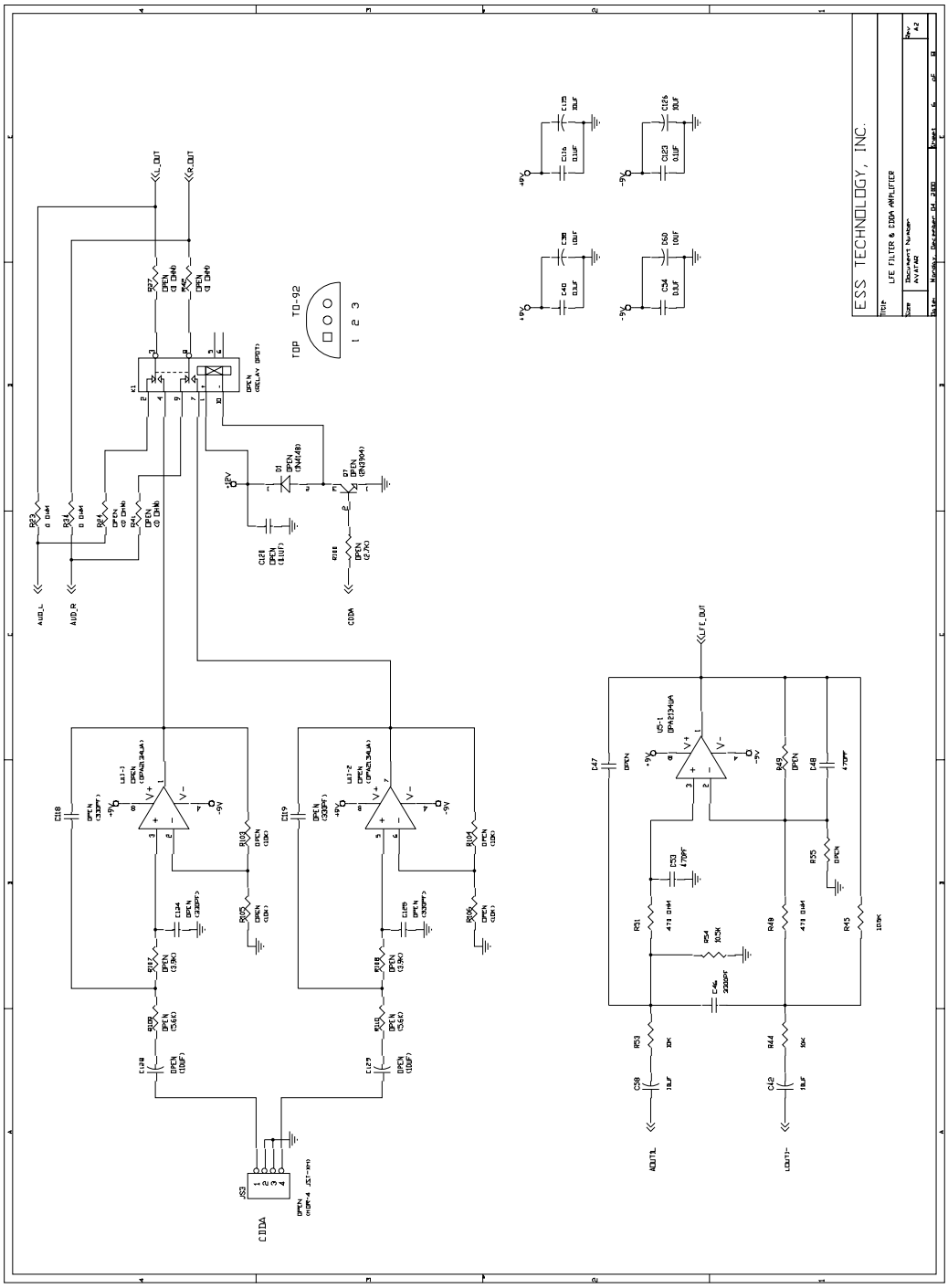


Figure 63 LFE Filter and CD-DA Amplifier

APPENDIX E: DVD-AUDIO DAUGHTERBOARD BILL OF MATERIALS

Table 44 DVD-Audio Daughterboard Bill of Materials

Item	Qty	Location	Description
Capacitors, SMD			
1	34	C8, C10, C12, C14, C23, C24, C26, C27, C40, C52, C54, C56, C67, C69, C70, C74, C82, C96, C99, C100, C101, C109, C114, C116, C117, C123, C142, C143, C151, C158, C161, C167, C178, C188	CAP, CER, SMT, 0805, 0.1 µF, 10%, 25V, X7R
2	6	C140, C145, C159, C160, C168, C177	CAP, CER, SMT, 0805, 0.01 µF, 10%, 50V, Z5U
3	6	C16, C35, C36, C46, C76, C103	CAP, CER, SMT, 0805, 3300 pF, 10%, 25V, X7R
4	6	C43, C59, C63, C80, C86, C94	CAP, CER, SMT, 0805, 22 pF, 5%, 50V, NPO
5	4	C163, C172, C175, C183	CAP, CER, SMT, 0805, 56 pF, 5%, 50V, NPO
6	4	C157, C170, C180, C186	CAP, CER, SMT, 0805, 330 pF, 5%, 50V, NPO
7	4	C3, C9, C15, C25	CAP, CER, SMT, 0805, 100 pF, 5%, 50V, NPO
8	2	C97, C98	CAP, CER, SMT, 0805, 220 pF, 5%, 50V, NPO
9	17	C18, C19, C21, C22, C29, C30, C48, C53, C78, C81, C88, C105, C108, C162, C171, C174, C182	CAP, CER, SMT, 0805, 470 pF, 5%, 50V, NPO
10	3	C7, C62, C90	CAP, CER, SMT, 0805, 2700 pF, 10%, 25V, X7R
Capacitors, Through-Hole			
11	48	C1, C2, C4, C5, C13, C28, C31, C32, C33, C34, C37, C38, C39, C41, C42, C44, C45, C49, C50, C55, C58, C60, C61, C64, C66, C71, C73, C75, C79, C83, C84, C85, C87, C89, C92, C93, C95, C102, C106, C107, C110, C111, C112, C115, C121, C122, C126, C148	CAP, ALUM, RADIAL, 10 µF, 20%, 16V, 2-mm LS
12	3	C173, C181, C184	CAP, ALUM, RADIAL, 470 µF, 20%, 25V, 5-mm LS
13	6	C147, C153, C164, C165, C166, C176	CAP, ALUM, RADIAL, 100 µF, 20%, 25V, 2.5-mm LS
Resistors, SMD, 5%			
14	2	R74, R102	RES, SMT, 1210, 4.7Ω ±5%, 1/4W
15	3	R126, R128, R130	RES, SMT, 0805, 33Ω ±5%, 1/10W
16	16	R112, R113, R114, R115, R116, R117, R118, R120, R121, R122, R123, R124, R125, R127, R129, R133	RES, SMT, 0805, 75Ω ±5%, 1/10W
17	6	R40, R57, R61, R69, R78, R88	RES, SMT, 0805, 10Ω ±5%, 1/10W
18	6	R47, R59, R62, R72, R81, R91	RES, SMT, 0805, 100k Ω ±5%, 1/10W
19	1	R149	RES, SMT, 0805, 4.7k Ω ±5%, 1/10W
20	1	R93	RES, SMT, 0805, 18k Ω ±5%, 1/10W
21	2	R139, R150	RES, SMT, 0805, 1k Ω, ±5%, 1/10W
22	1	R83	RES, SMT, 0805, 560Ω ±5%, 1/10W
23	12	R8, R13, R26, R29, R31, R32, R48, R51, R67, R71, R89, R96	RES, SMT, 0805, 470Ω ±5%, 1/10W

Table 44 DVD-Audio Daughterboard Bill of Materials (Continued)

Item	Qty	Location	Description
Resistors, SMD, 5% (continued)			
24	2	R23, R34	RES, SMT, 0805, 0 Ω ±5%, 1/10W
Resistors, SMD, 1%			
25	23	R1, R2, R5, R6, R7, R10, R12, R14, R16, R19, R25, R30, R35, R37,R38, R39, R44, R53, R63, R70, R84, R86, R95	RES, SMT, 0805, 10k Ω ±1%, 1/10W
26	12	R3, R17, R28, R33, R36, R43, R45, R54, R64, R75, R80, R97	RES, SMT, 0805, 10.5k Ω ±1%, 1/10W
27	3	R22, R77, R99	RES, SMT, 0805, 499k Ω ±1%, 1/10W
Ferrites and Inductors			
28	4	FB3, FB5, FB7, FB8	FERRITE BEAD, AXIAL
29	4	L1, L4, L7, L10	INDUCTOR, 1 µH, AXIAL
30	4	L2, L5, L8, L11	INDUCTOR, 2.7 µH, AXIAL
31	4	L3, L6, L9, L12	INDUCTOR, 0.68 µH, AXIAL
Diodes			
32	8	D2, D3, D4, D5, D6, D7, D8, D9	DIODE, 1N6263, AXIAL
Transistors and Regulators			
33	1	U14	REG, 78M05, +5V, TO–220
34	1	U13	REG, 78M09, +9V, TO–220
35	1	U15	REG, 79M09, -9V, TO–220
Headers and Connectors			
36	1	JS1	HEADER, 1x2, 0.1-in. CENTERS, JST XHP-2
37	2	JS6, JS8	HEADER, 1x6, 0.1-in. CENTERS, JST XHP-6
38	1	JS4	HEADER, 1x4, 0.1-in. CENTERS, JST XHP-4
39	1	JS2	HEADER, 2x10, 0.1-in. CENTERS
40	1	P2	CONN, RCA, SINGLE, RT ANGLE, BOARD MOUNT
41	2	P5,P1	CONN, RCA, 6 CONN, RT ANGLE, BD MOUNT
42	1	P4	CONN, S-VIDEO, 4-PIN MIN DIN, RT ANGLE, BD MOUNT
IC Devices			
43	1	U10	IC, YSS903, YAMAHA, SO–28
44	1	U7	IC, AUDIO DAC, AK4356, AKM, QFP–44
45	7	U1, U2, U3, U4, U5, U8, U9	IC, OPAMP, DUAL, OPA2134, SO–8
46	1	U12	IC, DS75176BT, NATIONAL SEMI, SO–8
47	1	U16	IC, DS1233 TO–92
Miscellaneous			
48	1	P3	FIBER OPTIC TRANSMITTER, TOTX178, TOSHIBA
49	1	T1	TRANSFORMER, 6-PIN, 1:1, SCHOTT 67129600

APPENDIX F: DVD-AUDIO DAUGHTERBOARD GERBER FILES

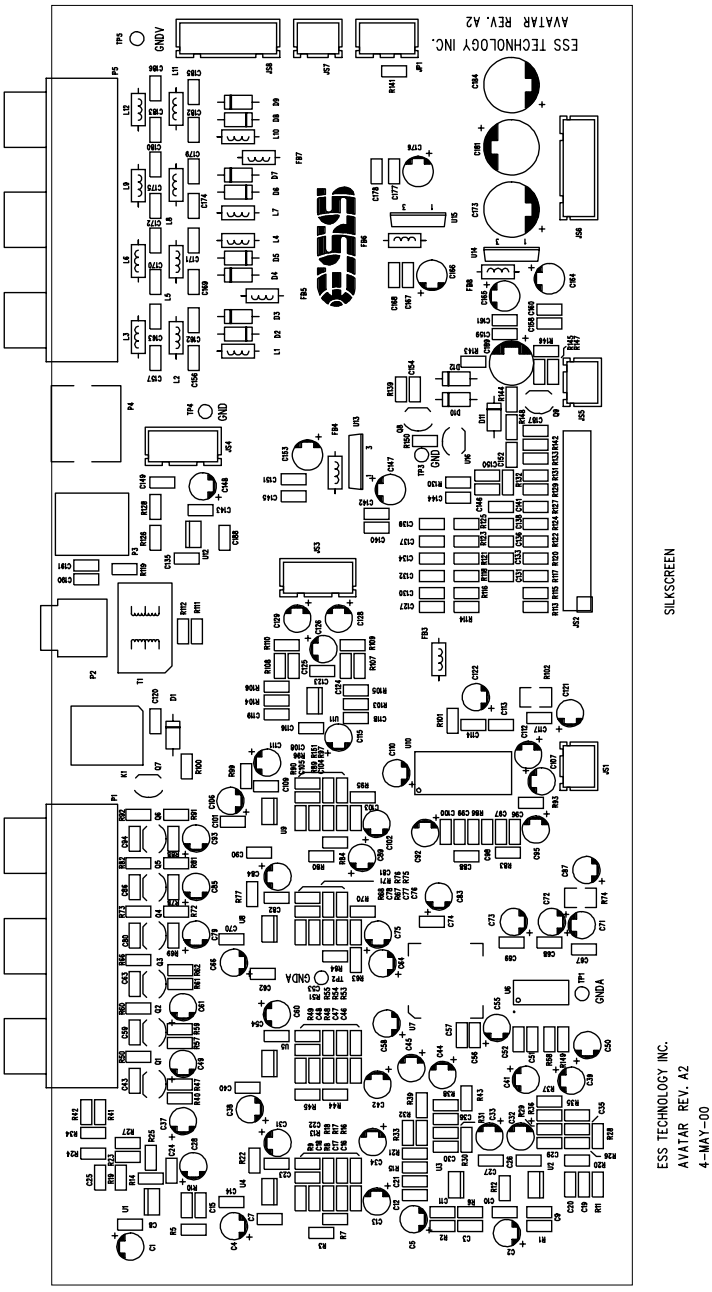


Figure 64 Daughterboard Silkscreen

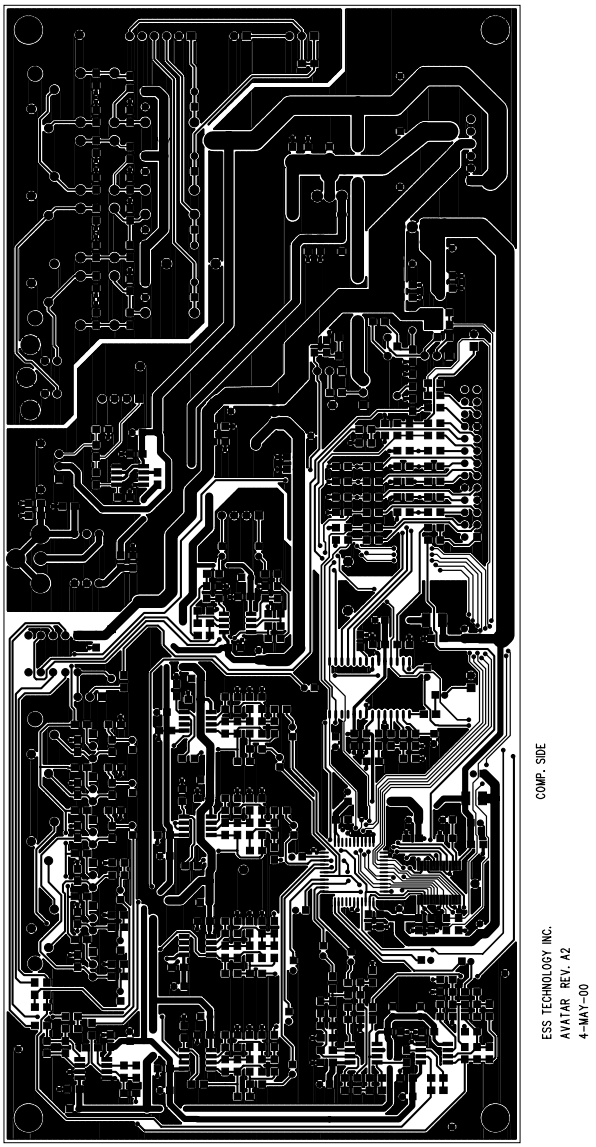


Figure 65 Daughterboard Top Layer

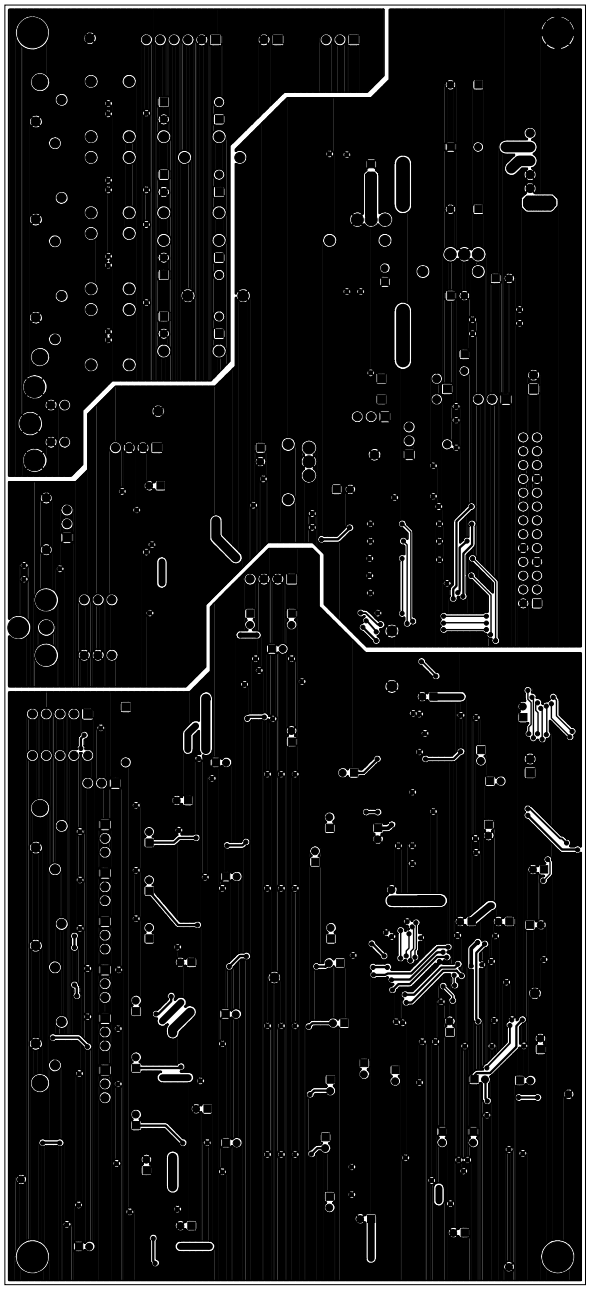


Figure 66 Daughterboard Bottom Layer

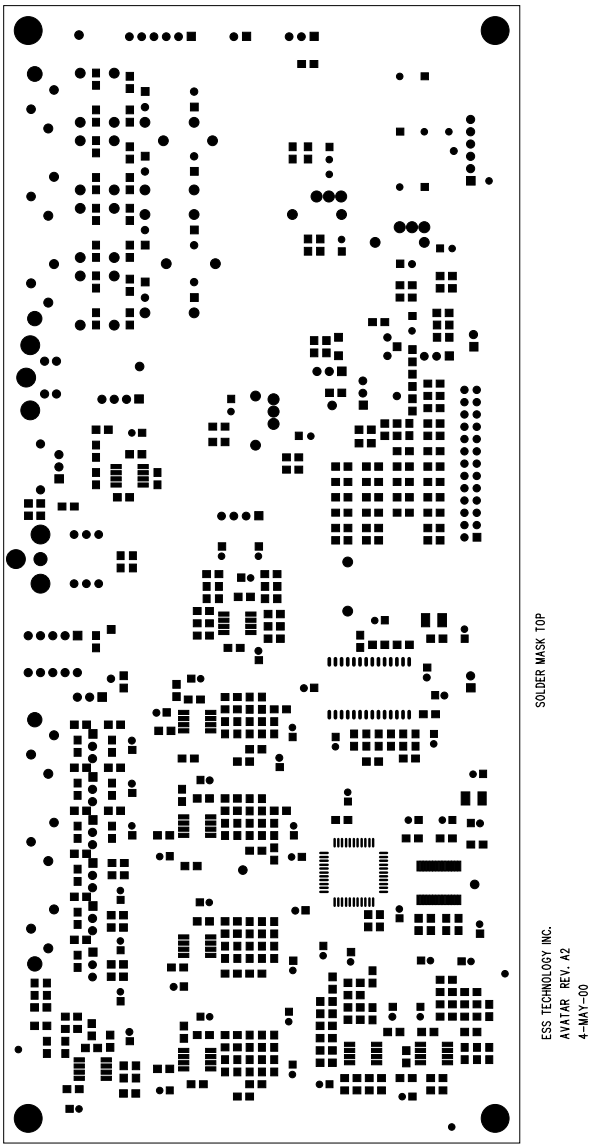


Figure 67 Daughterboard Solder Mask Top Layer

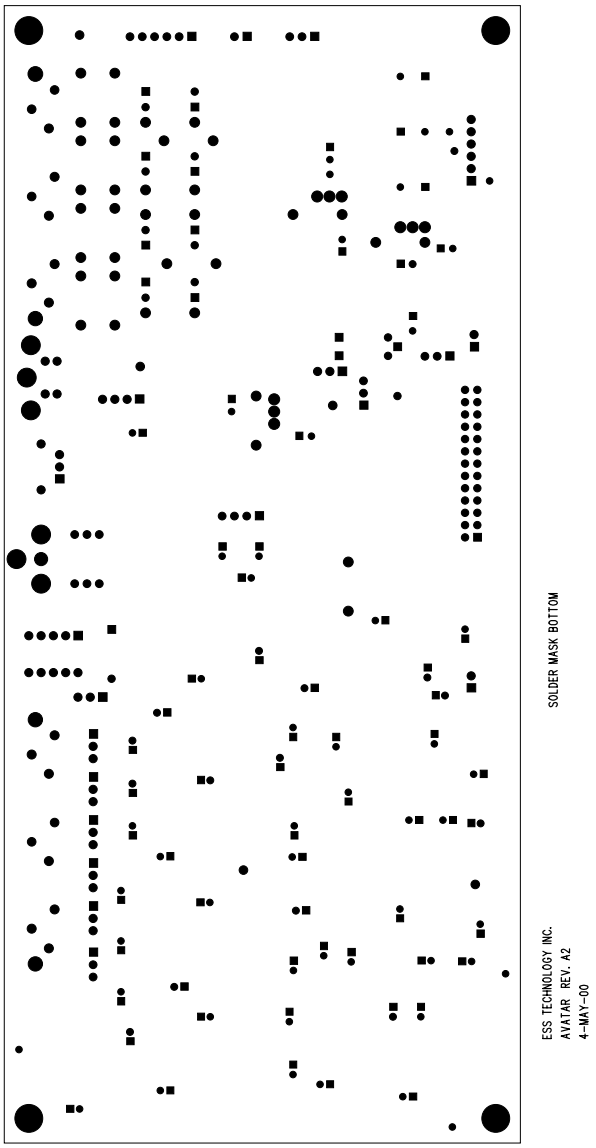


Figure 68 Daughterboard Solder Mask Bottom Layer

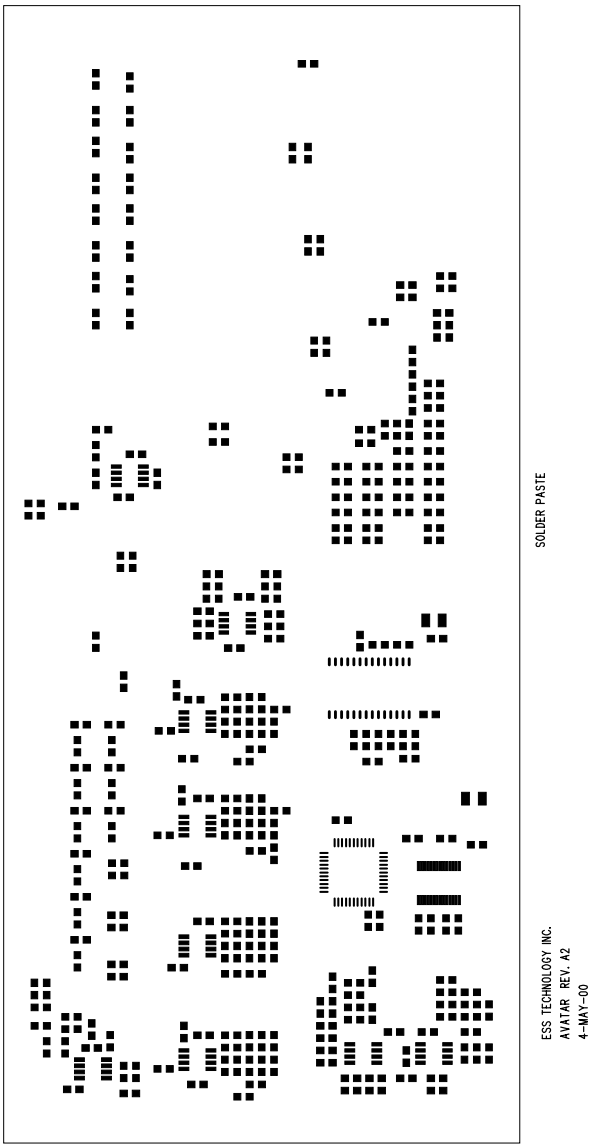


Figure 69 Daughterboard Solder Paste Top Layer

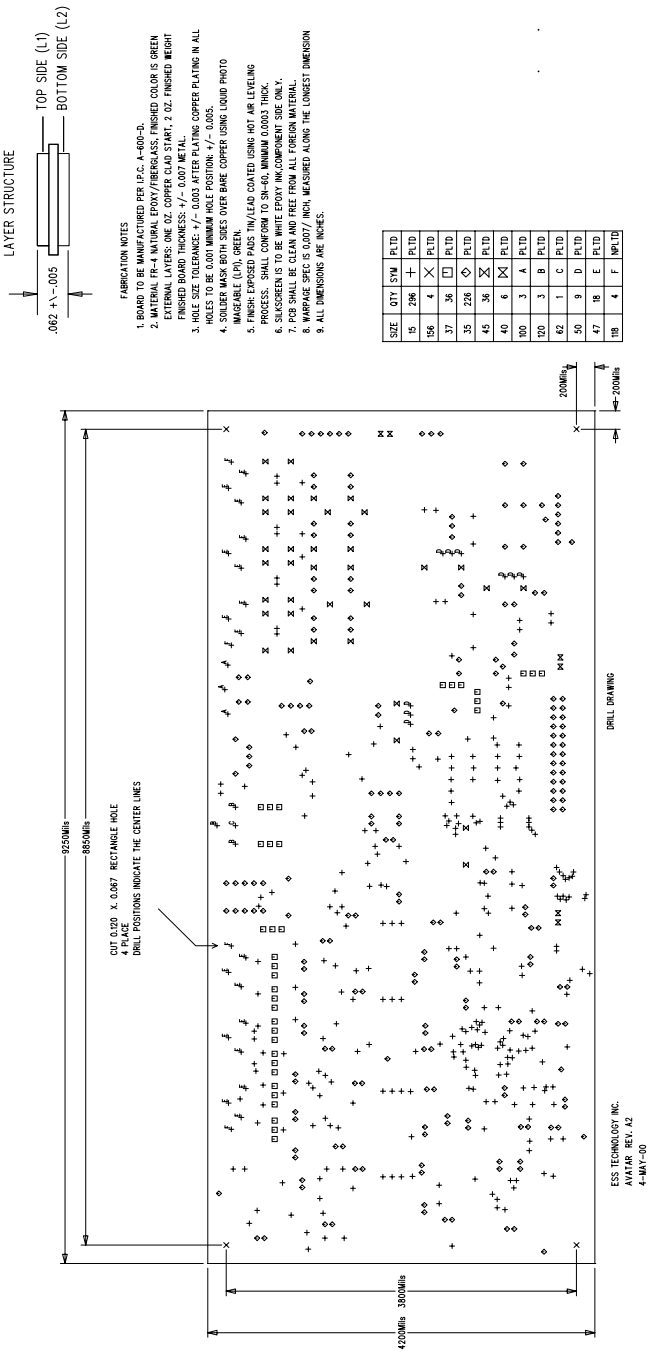


Figure 70 Daughterboard Drill Hole Template

APPENDIX G: VFD BILL OF MATERIALS

Table 45 VFD Bill of Materials

Item	Qty	Location	Description
Capacitors, 0805 SMD			
1	7	C8, C9, C11, C25, C27, C28, C30	CAP, CER, SMT, 0805, 0.1 µF, 10%, 25V, X7R
2	2	C13, C5	CAP, CER, SMT, 0805, 150 pF, 5%, 50V, NPO
Capacitors, Power			
3	6	C3, C4, C10, C12, C15, C18	CAP, ALUM, RADIAL, 1 µF, 20%, 25V, 2-mm LS
4	2	C1, C16	CAP, ALUM, RADIAL, 4.7 µF, 20%, 25V, 2-mm LS
5	1	C6	CAP, ALUM, RADIAL, 10 µF, 20%, 16V, 2-mm LS
6	4	C2, C7, C17, C26	CAP, ALUM, RADIAL, 47 µF, 20%, 16V, 2-mm LS
7	1	C29	CAP, ALUM, RADIAL, 47 µF, 20%, 35V, 3.5-mm LS
8	1	C14	CAP, ALUM, RADIAL, 22 µF, 20%, 16V, 2-mm LS
Resistors, SMD, 5%			
9	2	R1, R16	RES, SMT, 0805, 47 Ω, 5%, 1/10W
10	4	R2, R9, R10, R18	RES, SMT, 0805, 22k Ω, 5%, 1/10W
11	2	R3, R17	RES, SMT, 0805, 2.2k Ω, 5%, 1/10W
12	7	R4, R8, R14, R28, R29, R30, R31	RES, SMT, 0805, 10k Ω, 5%, 1/10W
13	2	R5, R15	RES, SMT, 0805, 220 Ω, 5%, 1/10W
14	2	R6, R13	RES, SMT, 0805, 12k Ω, 5%, 1/10W
15	1	R7	RES, SMT, 0805, 10 Ω, 5%, 1/10W
16	1	R32	RES, SMT, 0805, 56k Ω, 5%, 1/10W
17	6	R35, R36, R38, R39, R40, R43	RES, SMT, 0805, 4.7k Ω, 5%, 1/10W
Potentiometers			
18	2	R11, R12	POT, 50k Ω
IC Devices			
19	1	U6	IC,VFD CONT., NEC Upd16311, QFP-52
20	1	U7	IC, IR REC, TFMS5380
21	1	U1	IC, MIC AMP, BA7760F, SO-14
22	1	U2	IC, CMOS, HCF4069U, SO-14
Display			
23	1	U5	FLUORESCENT DISP, ZEC VFD28-0704
Diodes			
24	9	D1, D2, D5, D6, D7, D8, D9, D10, D11	DIODE, 1N4148, THROUGH-HOLE
Transistors			
25	2	Q1, Q2	TRANS, 2N7002LT1, SOT-23
Headers and Connectors			
26	1	JP1	HEADER, 1x2, 0.1-in. CENTERS
27	3	JS2, JS3, JS6	HEADER, 1x4, 0.1-in. CENTERS, JST XHP-4
28	1	JS8	HEADER, 1x8, 0.1-in. CENTERS, JST XHP-8

Table 45 VFD Bill of Materials (Continued)

Item	Qty	Location	Description
Headers and Connectors (continued)			
29	2	J1, J2	0.25-in. PHONE JACK
Switches			
30	34	S1, S2, S3, S4, S5, S6, S7, S8, S9, S10, S11, S12, S13, S14, S15, S16, S17, S18, S19, S20, S21, S22, S23, S24, S25, S26, S27, S28, S29, S30, S31, S32, S34, S35	SWITCH, PUSHBUTTON, SPST
Un-install Components			
31	1	S33	SWITCH, TOGGLE, SPDT, DIGIKEY (CKN1071-ND)
32	5	D12, D14, D15, D16, D17	LED, RADIAL, T1-3/4, 0.1-in. LS, RED
33	1	JS1	HEADER, 1x13, 0.1-in. CENTERS, LOCKING
34	1	R19	POT, 50k Ω
35	1	U3	FLUORESCENT DISP, SAMSUNG SVV-10MS08
36	1	U4	FLUORESCENT DISP, SAMSUNG SVV-07MS08
37	1	JS7	HEADER, 1x4, 0.1-in. CENTERS, JST XHP-4
38	1	JS5	HEADER, 1x6, 0.1-in. CENTERS, JST XHP-6

APPENDIX H: VFD GERBER FILES

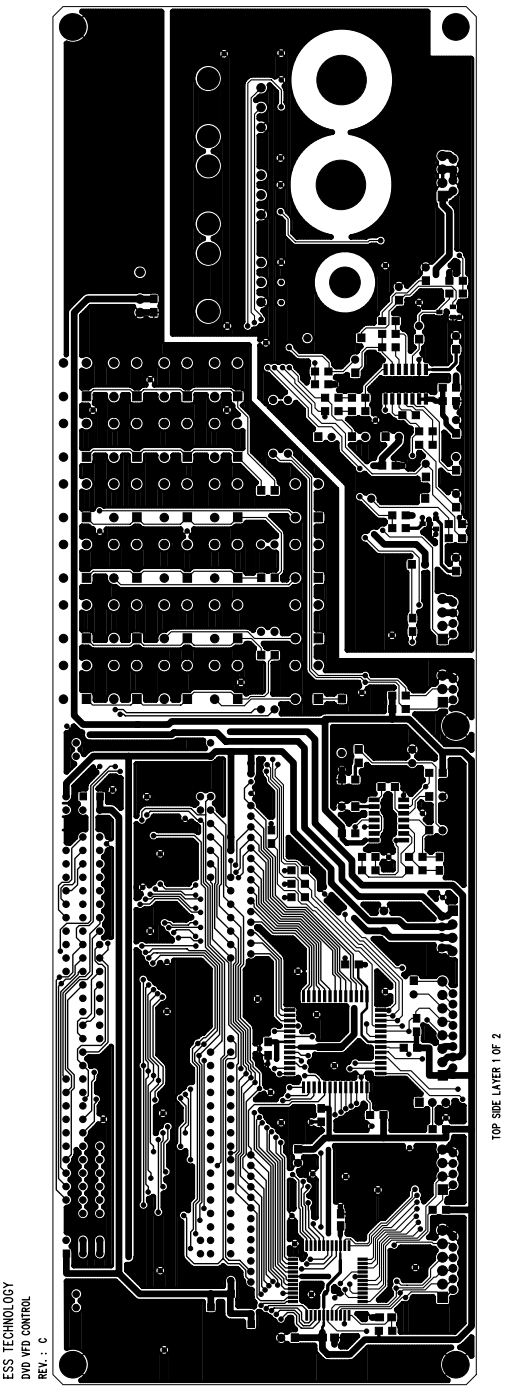


Figure 71 VFD Control Panel Top Layer

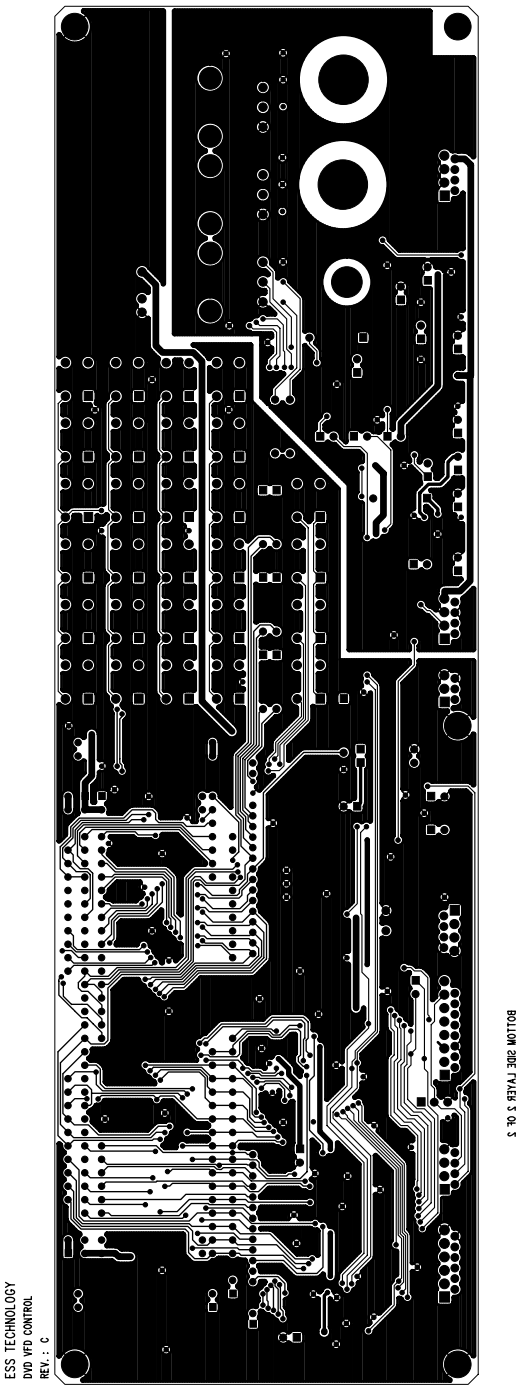


Figure 72 VFD Control Panel Bottom Layer

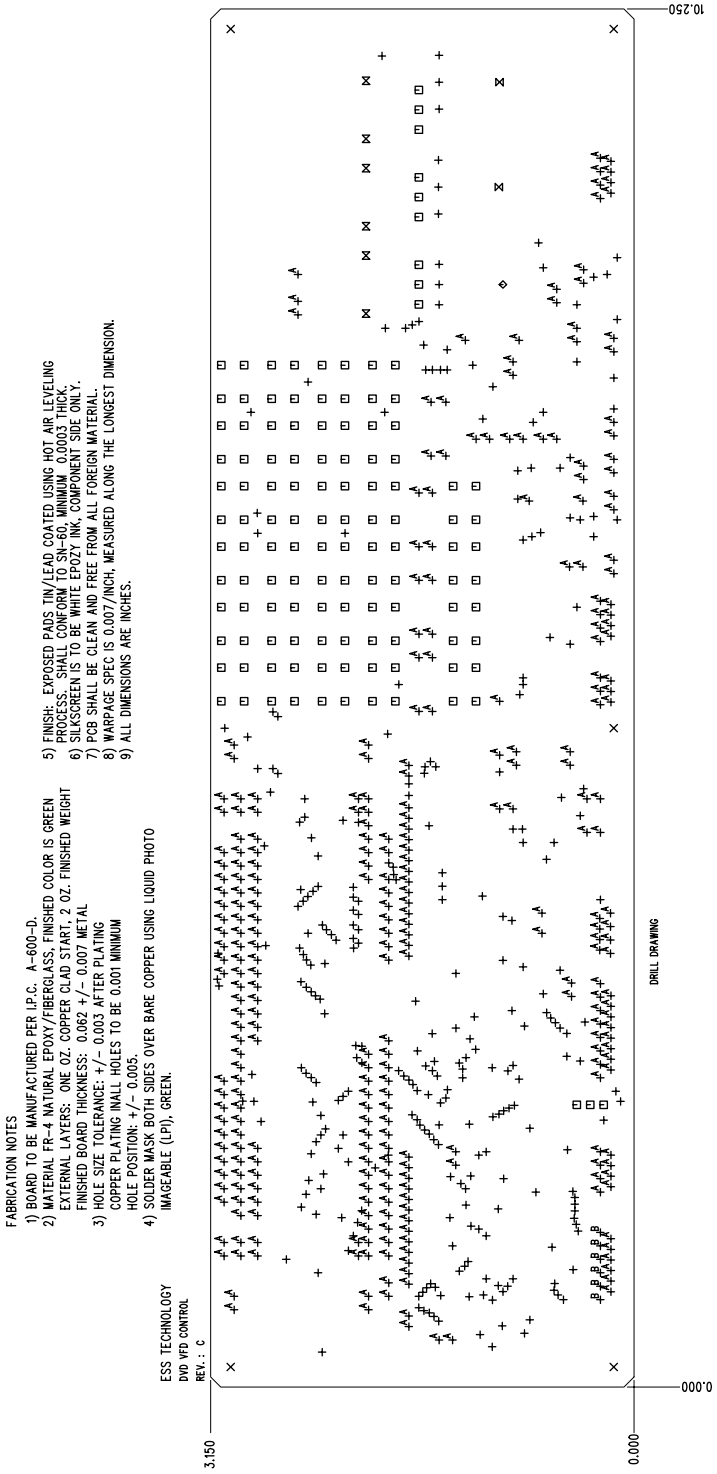


Figure 73 VFD Control Panel Drill Template

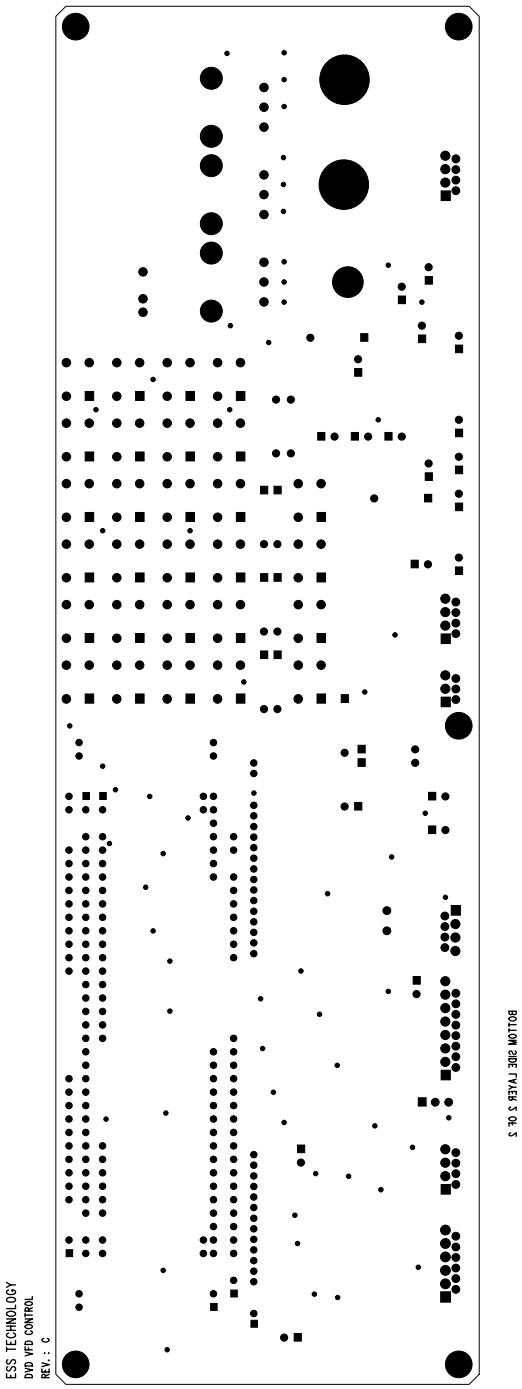


Figure 74 VFD Control Panel Solder Mask Bottom Layer

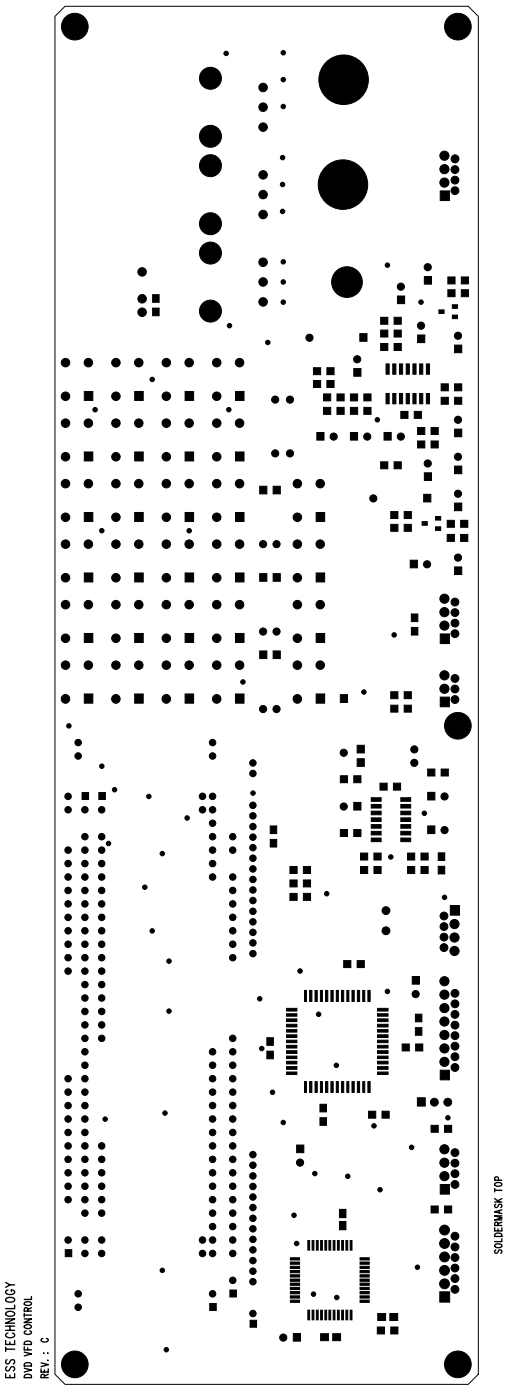


Figure 75 VFD Control Panel Solder Mask Top Layer

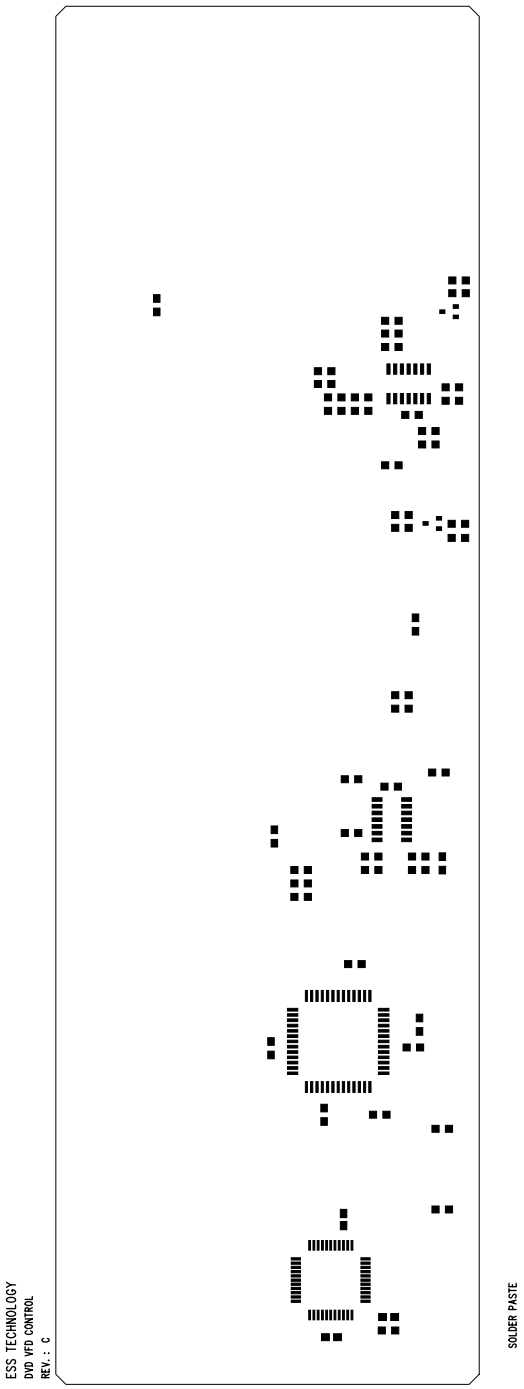


Figure 76 VFD Control Panel Solder Paste Layer

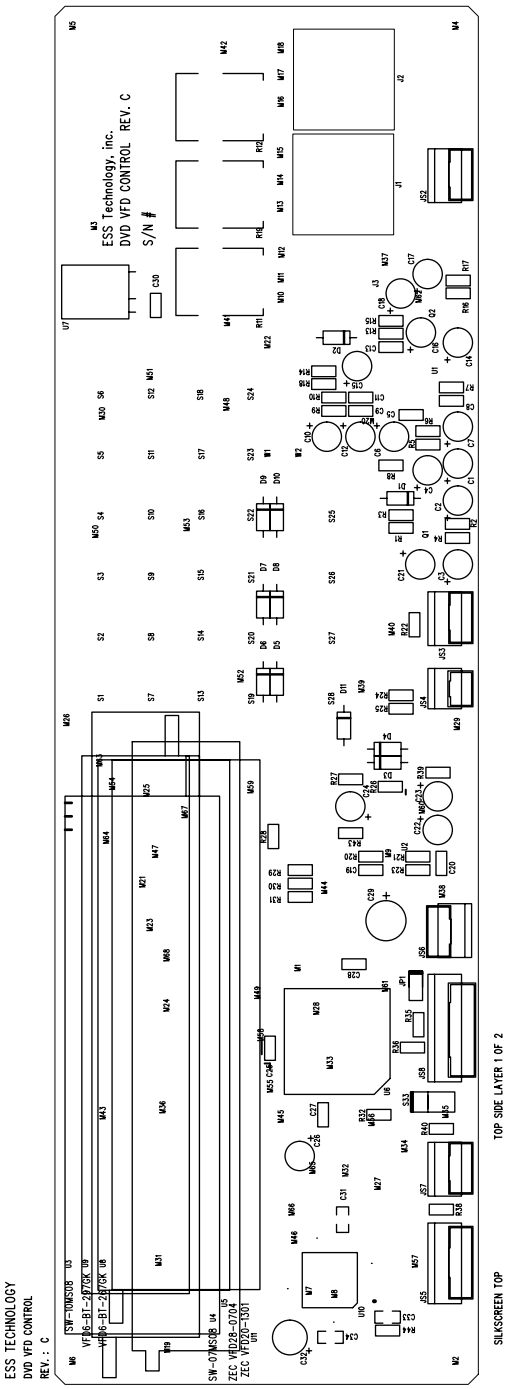


Figure 77 VFD Control Panel Silkscreen Layer

APPENDIX I: VFD CONTROL PANEL SCHEMATICS

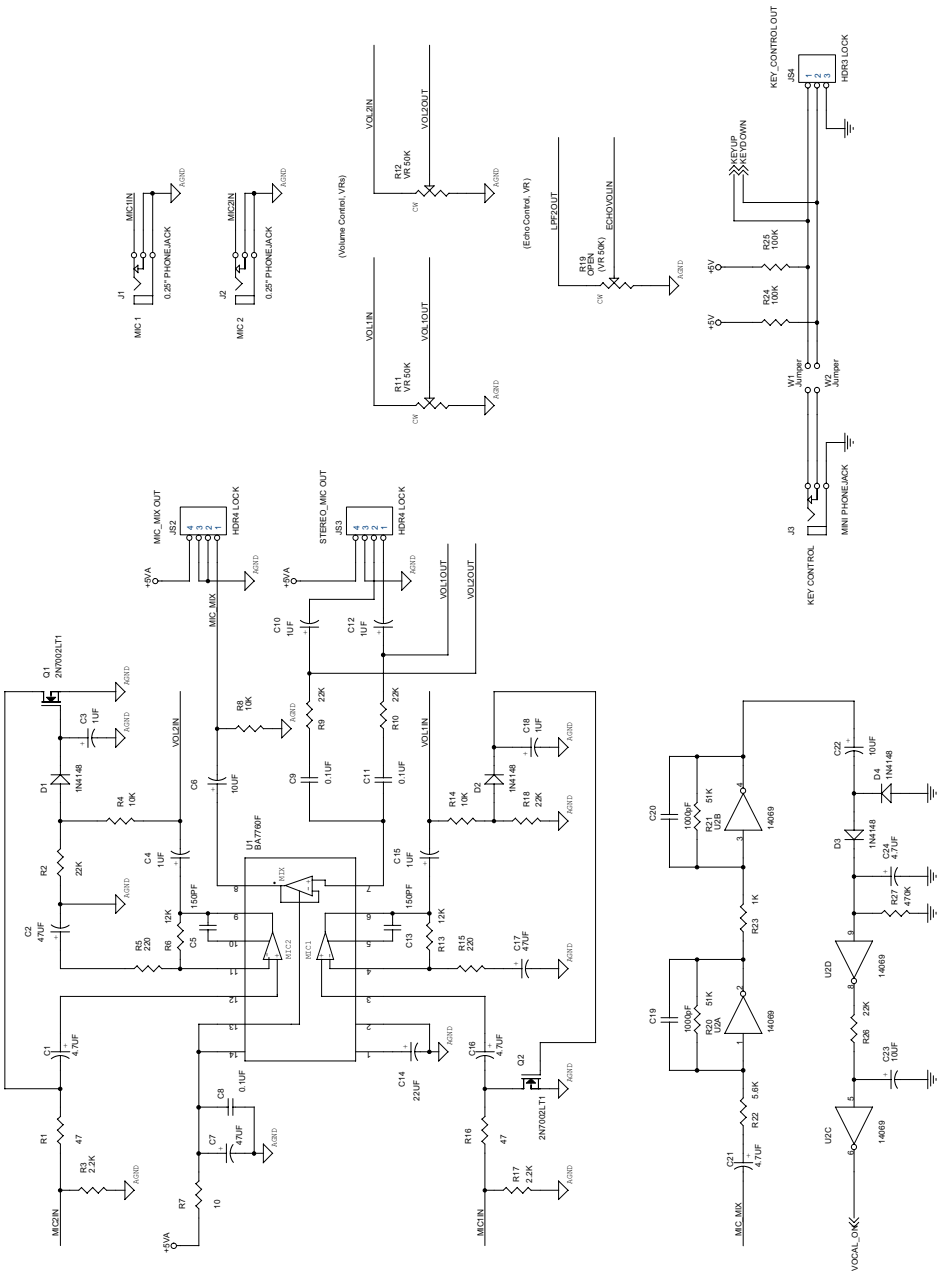


Figure 78 VFD Preamp

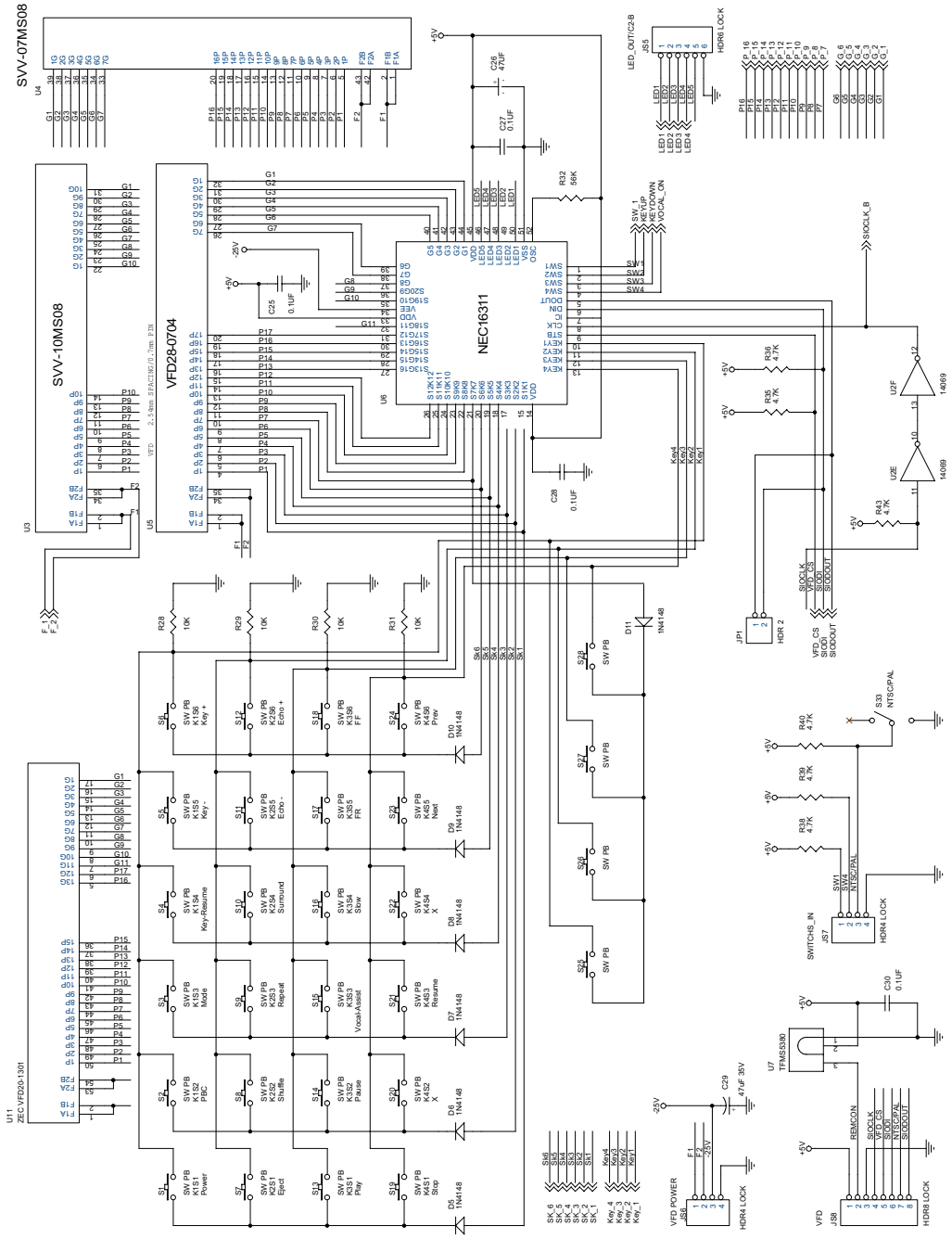


Figure 79 VFD Control Panel Switching Interface

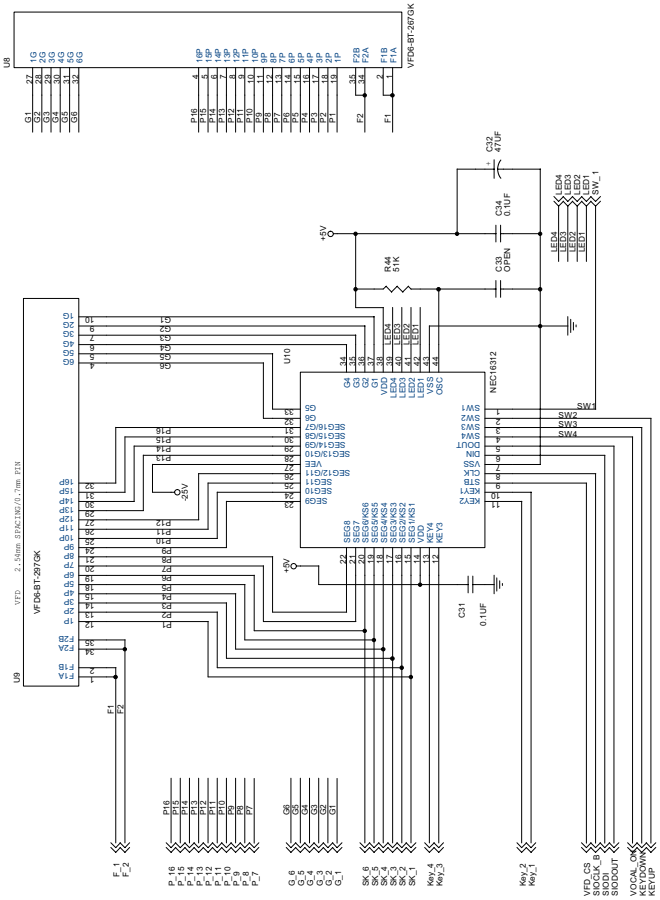
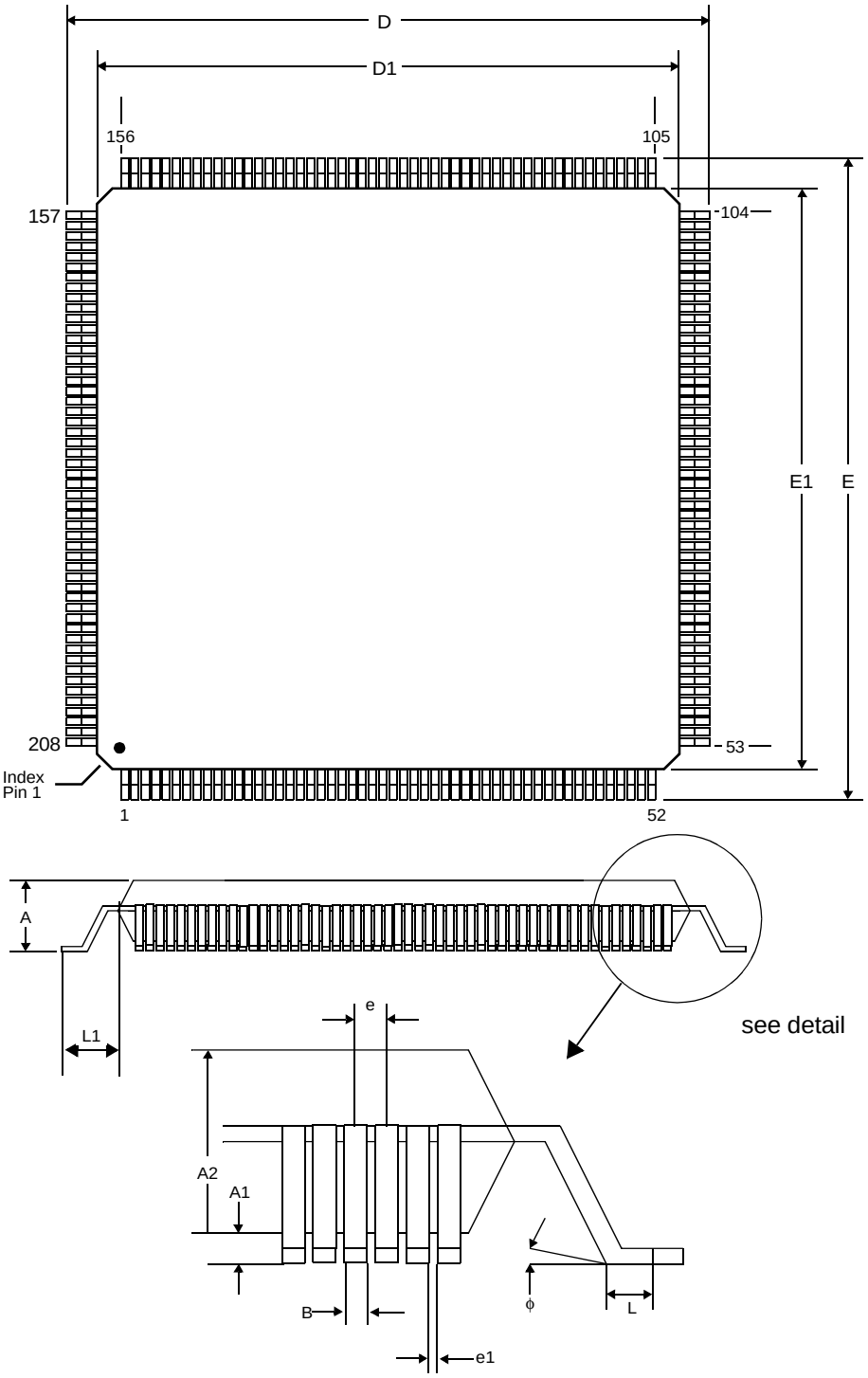


Figure 80 VFD Controller Interface

MECHANICAL DIMENSIONS



Note:
1. All dimensions are in millimeters.
2. Actual package uses millimeter native dimensions – care should be taken when converting from metric to imperial.

Symbol	Min	Nom	Max
A	3.42	3.70	4.09
A1	0.25	0.33	0.42
A2	3.17	3.37	3.67
B	0.13	0.17	0.27
D	30.35	30.60	30.85
D1	27.90	28.00	28.10
e	0.0197 (0.50) BASIC		
e1	0.20 BASIC		
E	30.35	30.60	30.85
E1	27.90	28.00	28.10
L	0.35	—	0.75
L1	—	1.30	—
ϕ	0°	—	7°

Figure 81 208-pin Plastic Quad Flat Package (PQFP)

ORDERING INFORMATION

Part Number	Description	Package
ES6008F	2-channel DVD and TV Encoder	208-pin PQFP
ES6018F	6-channel DVD, DTS and TV Encoder	208-pin PQFP
ES6028F	6-channel DVD, DTS, Progressive Scan and TV Encoder	208-pin PQFP
ES6038F	6-channel DVD, DTS, Progressive Scan, DVD-Audio and TV Encoder	208-pin PQFP

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