KasH Technology Inc.
TEL:886-3-5236508
FAX:886-3-5613221

Super Economic Digital Audio

KHTEK DA1134

24Bit, 192KHz Stereo Digital to Audio Converter

General Description

The DA1134 is a high-performance stereo digital to analog converter. The DA1134 supports the popular I^2S audio data format in 24bit at a sampling rate ranging from 16KHz to 192KHz. The DA1134 operates with a single 5V supply. The DA1134 requires minimal external supporting circuitry and is ideal for all consumer electronics applications such as, wireless speakers, Set-Top Box, VCD/SVCD player, DVD player, CD/DVD- ROM driver, MIDI applications, Karaoke system, etc.

Features

High Resolution:

16 Bit to 24 Bit I^2S Format

High Performance:

Sampling Rate: Up to 192KHz

THD+N: -85 dB

Dynamic Range: 102dB

S/N Ratio: 102dB

Channel Separation: 108dB

High Integration:

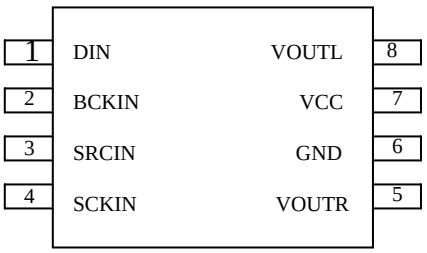
Over-sampling Digital Filter

High-Resolution Delta Sigma DAC

Analog Low Pass Filter

8 Pin SOP Package

Pin Configuration



Pin Assignments

Pin	Name	I/O	Description
1	DIN	IN	Audio Data Input
2	BCKIN	IN	Bit Clock Input for Audio Data
3	SRCIN	IN	Sample Rate Clock Input
4	SCKIN	IN	System Clock Input
5	VOUTR	OUT	R-Channel Output
6	GND	-	Analog Ground
7	VCC	-	Analog Power Supply
8	VOUTL	OUT	L-Channel Output

Absolute Maximum Rating

Power Supply Voltage	+ 6.5V
Input Logic Voltage	-0.3V to (VCC + 0.3V)
Power Dissipation	250mW
Operating Temperature Range	-25 ℃ to +85 ℃
Storage Temperature	-55 ℃ to +125 ℃

ESD Sensitive Device

Although DA1134 is furnished with KHTEK's proprietary ESD protection circuitry, proper ESD precaution is still recommended to avoid performance degradation or permanent damage.

Ordering Information

Part No.	Package	Package Drawing No.
DA1134	8 pin SOP	208-S
DA1134F	Lead Free 8 pin SOP	208-S

Package drawing is at the end of this data sheet

Specifications

Electrical Characteristics:

At 25°C, VCC=5V, 24Bit input data to produce 977Hz Sine Wave Output; fs=48kHz, System Clock = 256fs, Bit Clock = 64fs

Parameter	Conditions	Min	Type	Max	Unit
Sampling Frequency		16	48	192	KHz
System Clock Frequency			128/256/512 192/384/768		fs fs
Audio Data Format			IIS		
Data Bit Length		16		24	Bits
Power Supply **Voltage Range: VDD** **Supply Current: IDD** **Power Dissipation:**	 VDD=5V VDD=5V VDD=5V	 4.75	 5 15 75	 5.25 19 95	 V mA mW
Digital Input/Output **Input Logic Level** V_{IH} V_{IL}	 Pin1,2,3,4 --Schmitt Trigger	 54%		 28%	 VDD VDD
DC Accuracy **Gain Error** **Gain Mismatch Ch to Ch**			 +/- 1 +/- 1	 +/- 5 +/- 5	 %FSR %FSR
Analog Output Voltage Range Center Voltage Load Impedance Frequency Response	 VDD=5V, Vout=0dB AC Load 	 5 0	 60% 50% 	 20	 VDD VDD KOhm KHz

Electrical Characteristics (*Cont.*):

At 25°C, VCC=5V, 24Bit input data to produce 977Hz Sine Wave Output; fs=48kHz, System Clock = 256fs, Bit Clock = 64fs

Parameter	Conditions	Min	Type	Max	Unit
Dynamic Performance					
@fs=48KHz					
THD+N at FS(0dB)	RMS + A-weighted		-85	-80	dB
THD+N at –20dB	RMS + A-weighted		-78	-73	dB
THD+N at –60dB	RMS + A-weighted		-38	-33	dB
Dynamic Range	Average + A-weighted	97	102		dB
	RMS + CCIR2K	92	97		dB
SNR	Average + A-weighted	95	100		dB
	RMS + CCIR2K	92	97		dB
Channel Separation			108		dB
@fs=96KHz					
THD+N at FS(0dB)	RMS + A-weighted		-83	-78	dB
THD+N at –20dB	RMS + A-weighted		-78	-73	dB
THD+N at –60dB	RMS + A-weighted		-38	-33	dB
Dynamic Range	Average + A-weighted	97	102		dB
	RMS + CCIR2K	92	97		dB
SNR	Average + A-weighted	97	102		dB
	RMS + CCIR2K	92	97		dB
Channel Separation			108		dB
@fs=192KHz					
THD+N at FS(0dB)	RMS + A-weighted		-81	-76	dB
THD+N at –20dB	RMS + A-weighted		-79	-73	dB
THD+N at –60dB	RMS + A-weighted		-39	-33	dB
Dynamic Range	Average + A-weighted	97	102		dB
	RMS + CCIR2K	92	97		dB
SNR	Average + A-weighted	97	102		dB
	RMS + CCIR2K	92	97		dB
Channel Separation			108		dB

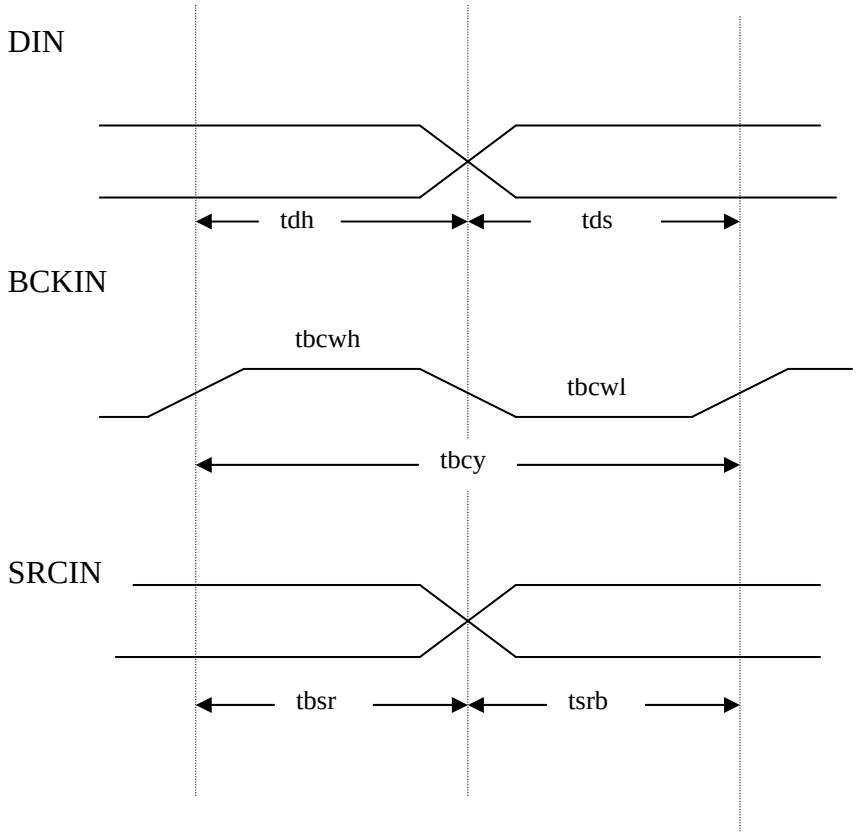
Timing Characteristics:

At 25°C, VCC=5V/3.3V, fs=48kHz, 24Bit input data, System Clock = 384/256fs

Data Input Timing			
Parameter	**Symbol**	**Value**	**Unit**
DIN setup time	tds	>30	ns
DIN hold time	tdh	>30	ns
BCKIN high-level, low-level	tbcwh, tbcwl	>50	ns
BCKIN pulse cycle time	tbcy	>100	ns
BCKIN rising edge to SRCIN	tbsr	>30	ns
SRCIN to BCKIN rising edge	tsrb	>30	ns

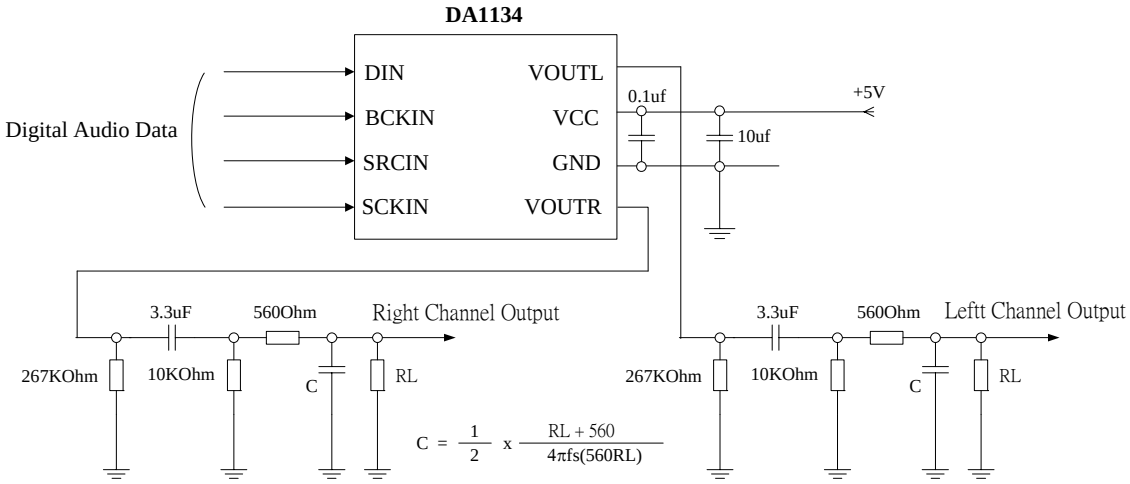
Timing Diagram

Data Input Timing:



Application Considerations

Application Circuit



System Clock

The system clock SCKIN (pin4) must be 128fs、 192fs、 256fs、 384fs、 512fs、 or 768fs, where fs is the standard audio frequency including 16KHz, 32KHz, 44.1KHz, 48KHz, 96KHz, and 192KHz.

Sampling Rate fs	System Clock (MHz)					
	128fs	192fs	256fs	384fs	512fs	768fs
16KHz	-	3.072	4,0960	6,1440	8.1920	12.2880
32 KHz	4.0960	6.1440	8.1920	12.2880	16.3840	24.5760
44.1 KHz	5.6448	8.4670	11.2896	16.9344	22.5792	33.8688
48 KHz	6.1440	9.2160	12.2880	18.4320	24.5760	36.8640
96 KHz	12.2880	18.4320	24.5760	36.8640	49.1520	73.7280
192KHz	24.5760	36.8640	-	-	-	-

Bypassing Power Supply

The great care should be taken for the power and grounding to achieve the highest performance possible. The power VCC (pin 7) should be connected to a clean 5V supply and the GND (pin 7) should be connected to the analog ground plane near by the device. A 0.1uf ceramic capacitor in parallel with a 10uF capacitor can be used for bypassing the power supply. The bypass capacitors should be located on the same layer as the device and as close as possible to the device with the smaller capacitor being the closest.

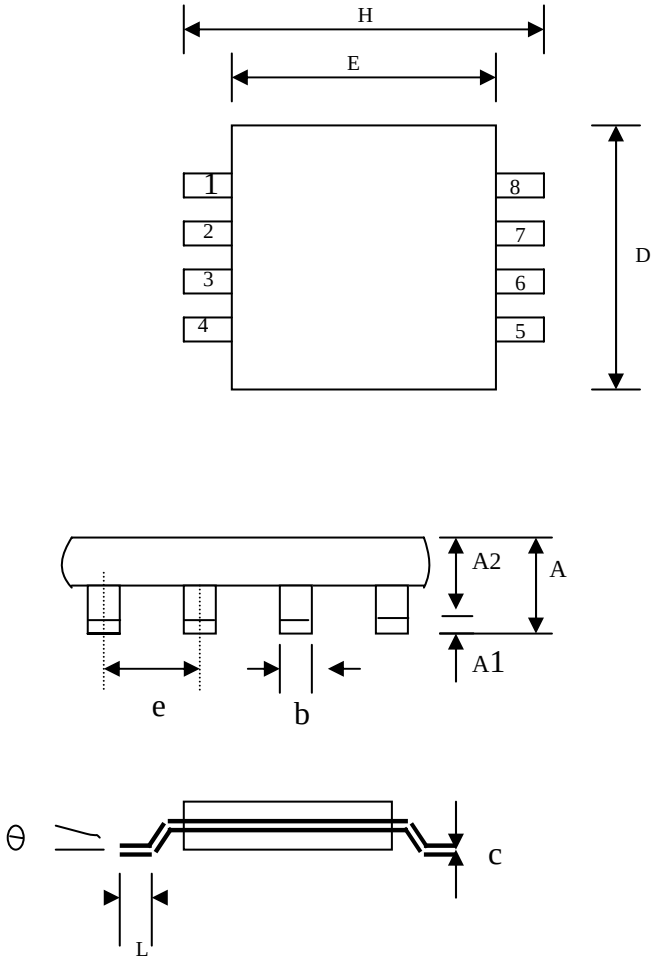
Output Filtering

To limit out of band noise, an external low pass filter as shown in the application circuit diagram is recommended, especially when the chip is to drive a wide band amplifier.

Package Drawing No. 208-S

Model	Package	Package Drawing No.
DA1134	8 pin SOP	208-S

Package outline drawing is shown as below:



Symbols	Dimensions in millimeters			Dimensions in inches		
	Min	Nom	Max	Min	Nom	Max
A	1.35	1.60	1.75	0.053	0.063	0.069
A1	0.10	----	0.25	0.004	----	0.010
A2	----	1.45	----	----	0.057	----
b	0.33	0.41	0.51	0.013	0.016	0.020
c	0.19	0.20	0.25	0.007	0.008	0.010
D	4.8	8.64	5.0	0.189	0.340	0.197
H	5.80	5.99	6.20	0.228	0.236	0.244
E	3.80	3.91	4.00	0.150	0.154	0.157
e	-----	1.27	----	----	0.050	----
L	0.40	0.71	1.27	0.016	0.028	0.050
θ	0^o		8^o	0^o		8^o