Preliminary Specification
CS801-B-I

iNTEGRATED MEMORY LOGIC

8 Channel Programmable Gamma and VCOM Buffer with 2 Bank Memory

General Description

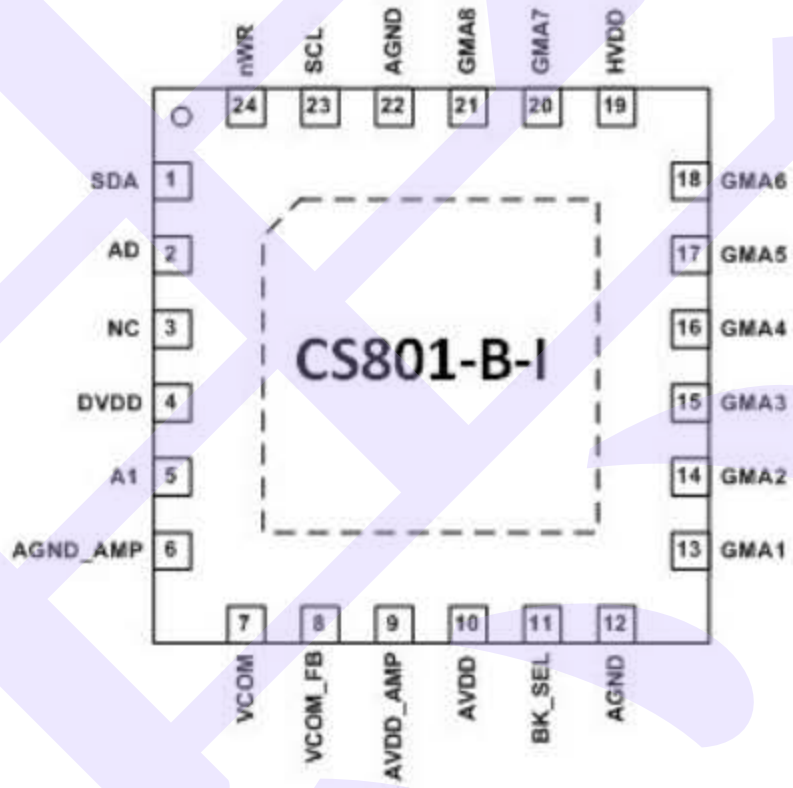
The CS801-B-I is an I^2C LCD programmable digital gamma buffer and digital voltage reference. It has 8 channels of programmable reference voltage generators with 1 voltage reference for VCOM. The VCOM reference voltage and each gamma reference voltage has its own 10-bit digital-to-analog converter (DAC) and buffer to ensure a stable voltage output. The VCOM reference voltage also has its own amplifier for stable voltage when critical levels and patterns are displayed. The CS801-B-I also features an integrated EEPROM memory, configured as two selectable banks, and memory interface, making the EEPROM interface transparent to the user. The EEPROM supports up to 10,000 write operations. and eliminates the need for external EEPROM. The two selectable bank configuration allows storage of two sets of gamma data and VCOM data allowing dynamic switching between two different gamma curves. The CS801-B-I provides a complete 8-channel gamma solution for TFT-LCD displays.

Each gamma output can drive 200mA peak transient current and the VCOM output can drive 400mA peak transient current. The analog supply voltage range extends from 9V to 20V and the digital supply voltage range extends from 2.7V to 3.6V.

The VCOM and Gamma values are programmed into registers through the I^2C interface.

The CS801-B-I is available in a 24-pin (4x4) TQFN thermally enhanced package.

Pin Diagram (Top View)



Features

- 8 Channel Programmable Gamma Correction
- 10-bit Programmable Built-in Reference
- Integrated EEPROM Memory with Two Selectable Banks
- 1 channel programmable VCOM buffer
- Programmable VCOM Limits
- Programmable VCOM gain
- HVDD supplies to reduce power consumption
- Exposed thermal pad package to reduce temperature
- 20V Maximum analog Supply voltage

Ordering Information

Package	Part Number	Tape & Reel
24-pin TQFN (Halogen Free)	CS801-B-I	13"

Applications

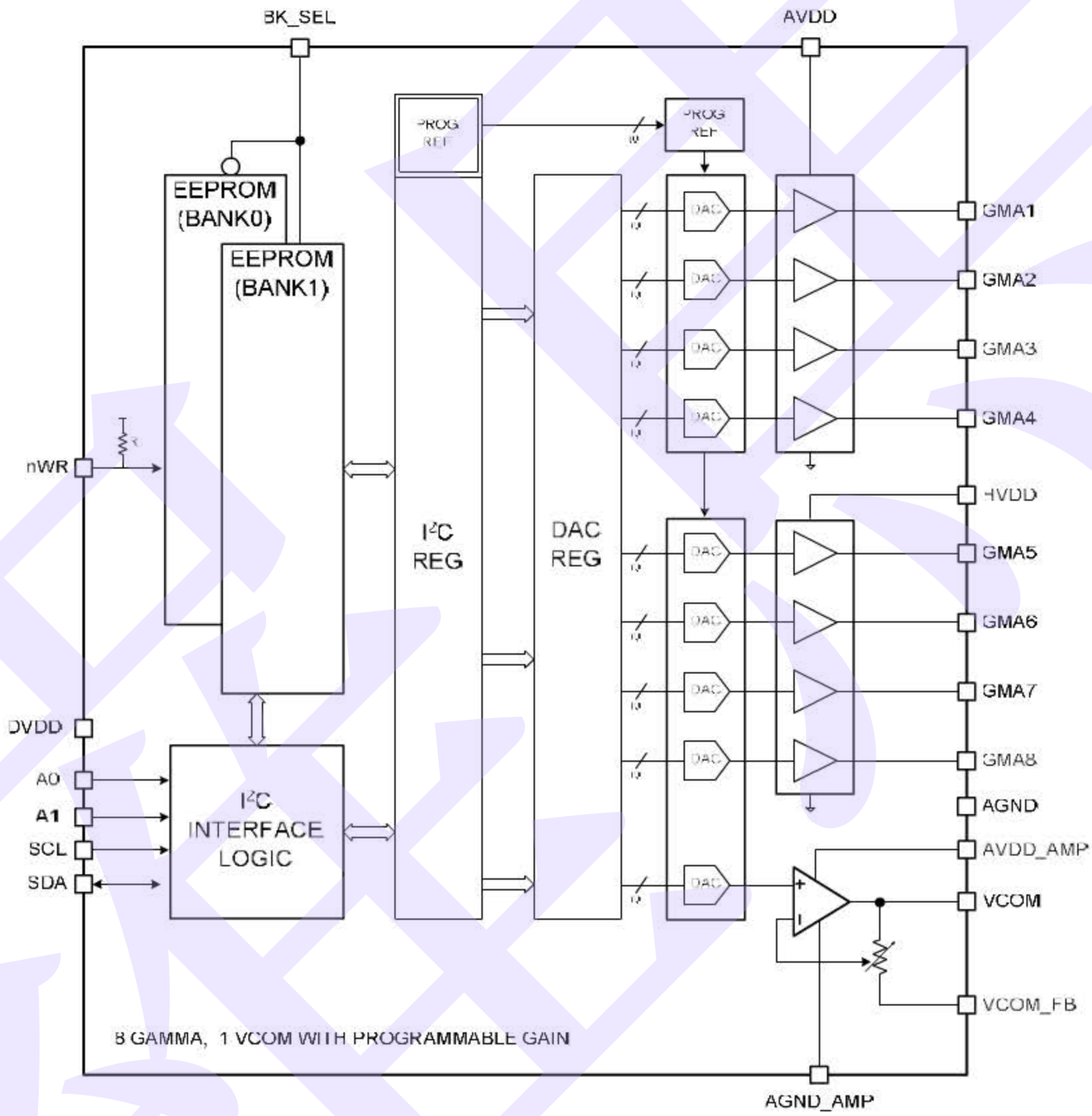
- TFT-LCD TVs
- TFT-LCD Monitors
- TFT-LCD Notebook PC
- Reference Voltage Generators

Pin Descriptions

Pin No.	Pin Name	Function
1	SDA	I^2C Compatible Serial-Data Input/Output
2	A0	I^2C Compatible Device Address Bit 0
3	NC	No Connection
4	DVDD	Digital Power Supply
5	A1	I^2C Compatible Device Address Bit 1
6	AGND_AMP	Ground for VCOM Amplifier
7	VCOM	VCOM Output
8	VCOM_FB	Feedback for VCOM Amplifier
9	AVDD_AMP	Power Supply for VCOM Amplifier.
10	AVDD	Analog Power Supply
11	BK_SEL	Bank Select to select memory bank to be programmed. **Bank 0: BK_SEL=0** **Bank 1: BK_SEL=1**
12	AGND	Analog Ground
13	GMA 1	Gamma DAC Analog Output 1
14	GMA 2	Gamma DAC Analog Output 2
15	GMA 3	Gamma DAC Analog Output 3
16	GMA 4	Gamma DAC Analog Output 4
17	GMA 5	Gamma DAC Analog Output 5
18	GMA 6	Gamma DAC Analog Output 6
19	HVDD	Half VDD Supply Voltage
20	GMA 7	Gamma DAC Analog Output 7
21	GMA 8	Gamma DAC Analog Output 8
22	AGND	Analog Ground
23	SCL	I^2C Compatible Serial Clock Input
24	nWR	Enable/Disable data write in Non Volatile Memory. (Note 1) nWR = 0 (LOW), Data can be written to Non Volatile Memory. nWR = 1 (HIGH), Data cannot be written to Non Volatile Memory.

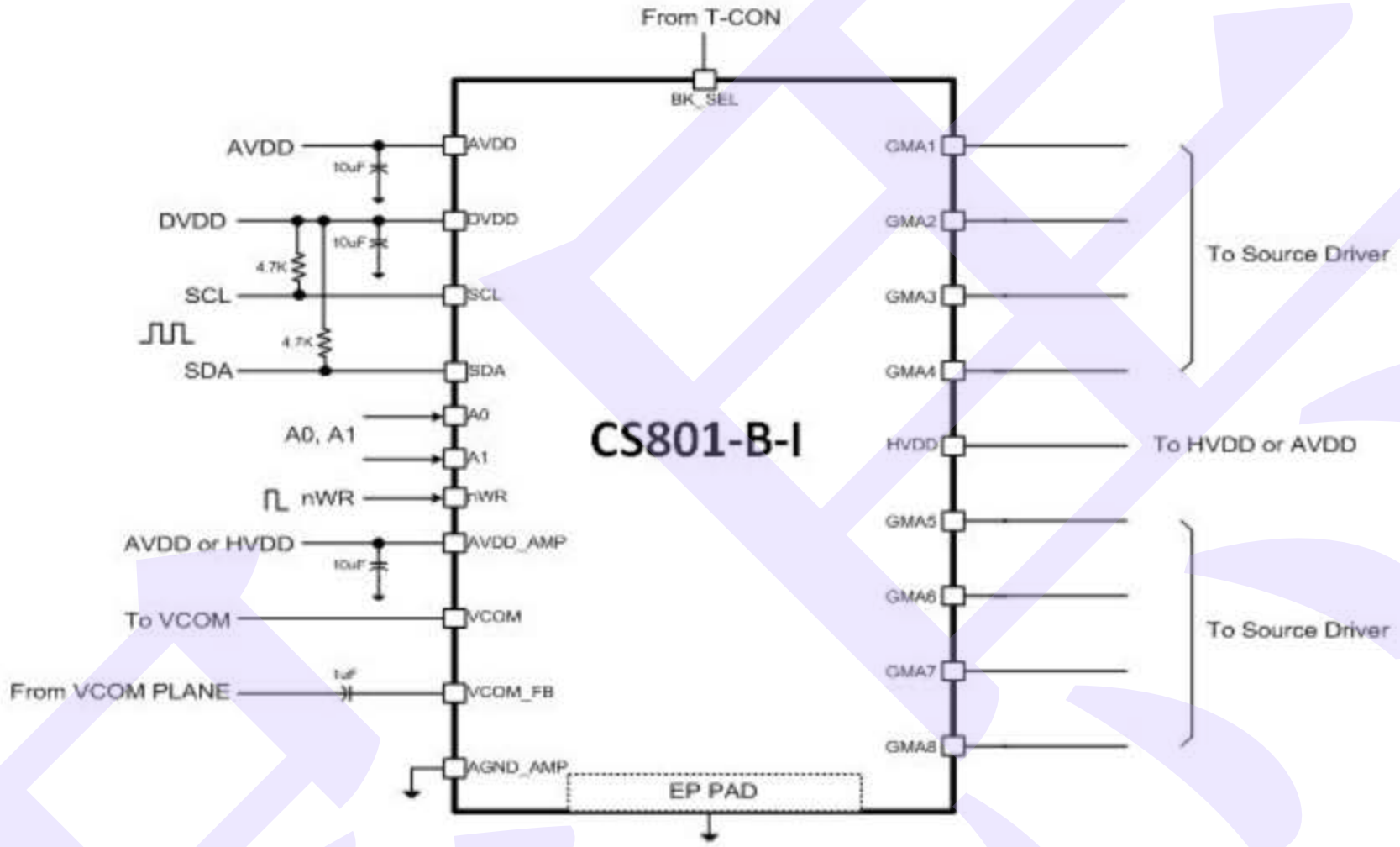
Note 1: The nWR pin is internally pulled HIGH through a pull up resistor, i.e. by default nWR = 1. Therefore it is not neccessary to pull this pin high externally. This PIN needs to be pulled LOW (=0) externally only when data need to be written to Non Volatile Memory,

Block Diagram

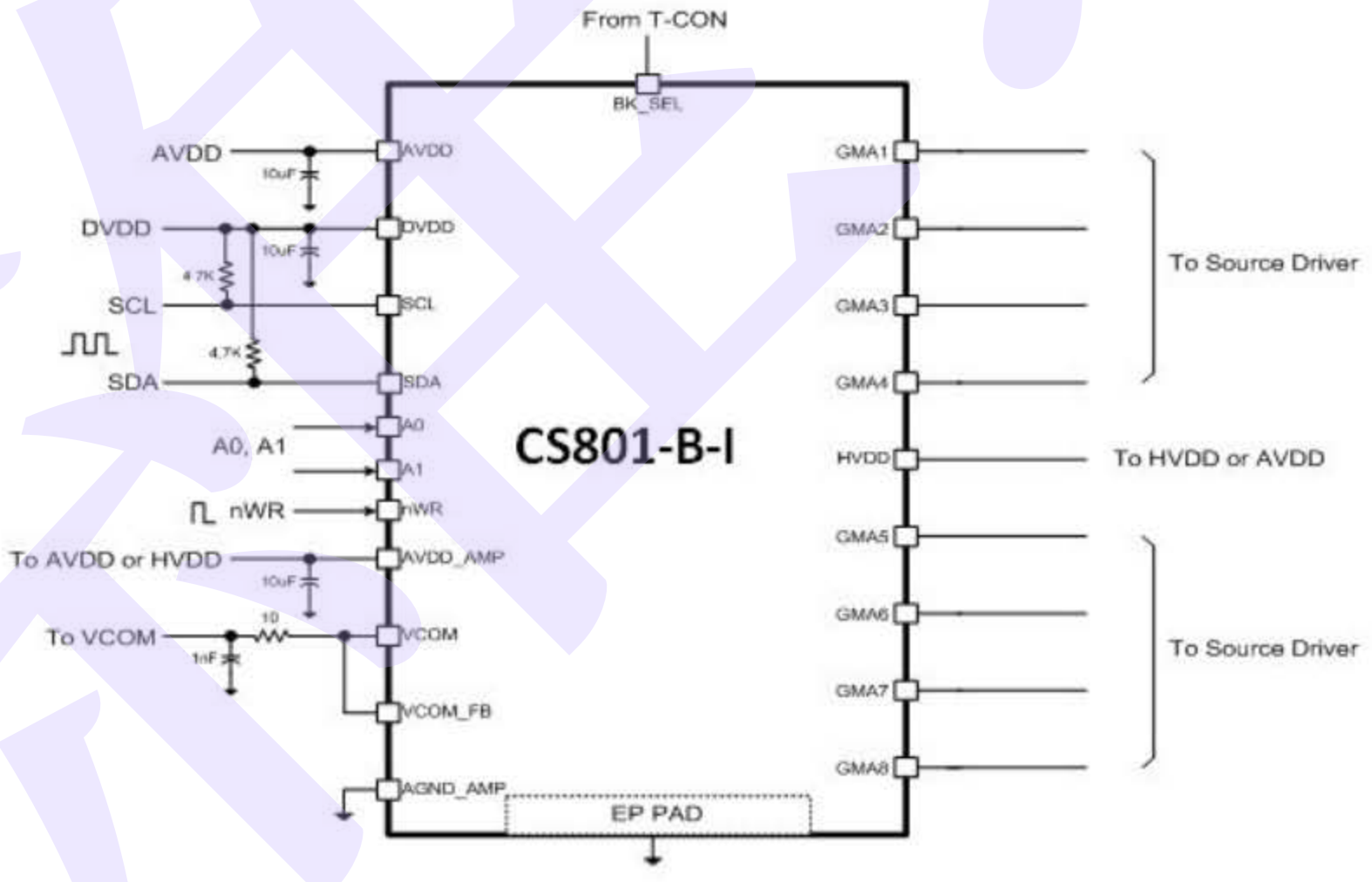


Typical Application Circuit

Internal Adjustable Gain Mode for VCOM



Unity Gain Mode for Half-Vdd



Absolute Maximum Ratings

Caution: Values beyond absolute ratings can cause the device to be prematurely damaged.
Absolute maximum ratings are stress ratings only and functional device operation is not guaranteed.

Maximum Voltages			
AVDD, HVDD to GND	- 0.3V to + 22V	**SDA, SCL**	+/- 10mA
AVDD_AMP to AGND_AMP	- 0.3V to + 22V	**GMA1-GMA8 (Maximum)**	+/- 200mA
DVDD to GND	- 0.3V to **+6.0V**	**VCOM (Maximum)**	+/- 400mA
AGND_AMP to GND	- 0.1V to +0.1V	**Continuous Power Dissipation (Ta=70 °C)**	2500mW
GMA1 – GMA4	HVDD - 0.3V to AVDD+0.3V	**Operating Temperature**	-40°C to +85°C
GMA5 – GMA8	- 0.3V to HVDD+0.3V	**ESD Rating: Device**	HBM: ±2KV
VCOM	- 0.3V to AVDD_AMP +0.3V	**Max. Lead Temperature (Soldering 10sec, Lead tips only)**	+260°C
VCOM_FB	- 0.3V to AVDD_AMP +0.3V	**Max. Storage Temperature Range**	-65°C to +150°C
SDA, SCL	- 0.3V to +4.5V	**Max. Junction Temperature**	+150°C

Electrical Characteristics

Test Conditions: V_{AVDD} = 18V, V_{AVDD_AMP} = 18V V_{DVDD} = 3.3V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are @T_A = 25°C. All parameters having Min/Max specifications are guaranteed. Typical values are for reference only. Unless otherwise noted, all tests are pulsed tests at the specified temperature, therefore: $T_J = T_C = T_A$..

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
DC CHARACTERISTICS						
Analog Supply Voltage Range	V_{AVDD}, V_{AVDD_AMP}, V_{HVDD}		9	18	20	V
Digital supply voltage	V_{DVDD}	Operating Voltage	2.7		3.6	V
		EEPROM Write	2.7			V
		EEPROM Read		2.5		V
Analog Quiescent Current	I_{AVDD}	HVDD=18V		8	10	mA
VCOM Quiescent Current	I_{AVDD_AMP}			5	7.5	mA
Digital Quiescent Current	I_{DVDD}			150	400	uA
Thermal Shutdown	TSD			+160		°C
Thermal Shutdown Hysteresis	$TSD_{(Hys)}$			15		°C
Under voltage Lockout Threshold	UVLO	DVDD under voltage lockout voltage threshold		2.3		V
VCOM OUTPUT (VCOM)[3], HALF AVDD OUTPUT (HAVDD)						
Resolution	RES		10			Bits
Integral Non-linearity Error	INL	T_A = +25°C 16 ≤ Code ≤ 1008		0.5		LSB
Differential Non-linearity Error	DNL	T_A = +25°C 16 ≤ Code ≤ 1008		0.5		LSB
Output Voltage Low	V_{outL}	T_A = +25°C, sinking 10mA, Referred to lower supply rail		0.15	0.3	V
Output Voltage High	V_{outH}	T_A = +25°C, sourcing 10mA Referred to upper supply rail	-0.3	-0.15		V
Output Load Regulation	LR	-5mA ≤I_{LOAD}≤ +5mA, Code = 512		±0.5		mV/mA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Short Circuit Current	I_{sc}	Output connected to either VCOM amplifier supply		400		mA
Total Output Error	V_{ERR}	Code = 512 V_{AVDD_AMP} = 9V and 18V T_A = +25°C	-10		10	mV
Slew Rate	SR	Swing 4Vp-p at VCOM, 10% to 90% R_l = 10kΩ, C_L = 50pF (note 3)		50		V/us
Bandwidth		R_l =10KΩ, C_l =50pF		20		MHz
GAMMA OUTPUTS						
Integral Non-linearity Error	INL	T_A = +25°C 16 ≤ Code ≤ 1008		0.5		LSB
Differential Non-linearity Error	DNL	T_A = +25°C 16 ≤ Code ≤ 1008		0.5		LSB
Total Output Error	V_{ERR}	Code = 512 V_{AVDD} = 9V and 18V T_A = +25°C		TBD		mV
Output Voltage Low	V_{outL}	T_A = +25°C, sinking 10mA, Referred to lower supply rail		0.15	0.3	V
Output Voltage High	V_{outH}	T_A = +25°C, sourcing 10mA Referred to upper supply rail	-0.3	-0.15		V
Output Load Regulation	LR	-5mA ≤I_{LOAD}≤ +5mA, Code = 512		±0.5	1.5	mV/mA
Output Resistance	ROUT	Buffer is disabled		120		KΩ
Short Circuit Current	I_{sc}	Outputs to AVDD or AGND		200		mA
PROGRAMMABLE REFERENCE (V_{REF})						
Full-Scale Voltage		Referred to output, T_A = +25°C	19.94	19.98	20	V
Resolution			10			Bits
Integral Non-linearity Error		T_A = +25°C 336 ≤ REF_Code ≤ 1007		0.5		LSB
Differential Non-linearity Error		T_A = +25°C 336 ≤ REF_Code ≤ 1007		0.5		LSB
LOGIC INPUTS (SDA, SCL, A0, A1, BK_SEL, nWR)						
Input High Voltage	V_{IH}		0.7 x V_{DVDD}			V
Input Low Voltage	V_{IL}				0.3 x V_{DVDD}	V
Input Leakage Current	I_{IH}, I_{IL}	V_{in} = 0 or V_{DVDD}	-10	0.01	10	uA
Input Capacitance				5		pF
Power Down Input Current	I_{IN}	V_{DVDD} = 0V, V_{IN} = 1.98V	-10		10	uA
SDA Output Low Voltage	V_{OL}	I_{SINK} = 3mA			0.4	V
I^2C INTERFACE						
SCL Clock Frequency	F_{SCL}				400	KHz
I^2C Clock High Time	t_{SCH}		0.6			µs
I^2C Clock Low Time	t_{SCL}		1.3			µs
I^2C spike rejection filter pulse width	t_{DSP}		0		50	ns
I^2C Data Set-up Time	t_{SDS}		100			ns
I^2C Data Hold Time	t_{SDH}		0		900	ns
I^2C SDA, SCL Input Rise Time	t_{I2CR}	Load dependent [4]	20 + 0.1*CB		300	ns

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
I^2C SDA, SCL Input Fall Time	t_{I2CF}	Load dependent [4]	20 + 0.1*CB		300	ns
I^2C bus free time between stop and start condition	t_{BUF}		1.3			µs
I^2C repeated start condition set-up time	t_{STS}		0.6			µs
I^2C repeated start condition hold time	t_{STH}		0.6			µs
I^2C Stop Condition Set-up	t_{SPS}		0.6			µs
I^2C Bus Capacitive Load	CB				400	pF

Note 2: All devices are 100% production tested at T_A = 25°C. All temperature limits are guaranteed by design.
Note 3: Measured with the VCOM amplifier configured as an inverting unity gain amplifier (R_S=R_F= 10kΩ).
Note 4: C_B is in pF.

Detailed Description

The CS801-B-I features 9 (8 gamma and 1 VCOM) programmable reference voltage channels. Each channel has a 10-bit DAC to create the reference voltage. The CS801-B-I features an integrated EEPROM memory, configured as two selectable banks supporting up to 10,000 write operations and eliminating the need for external EEPROM. The two selectable bank configuration allows storage of two sets of gamma and VCOM data allowing dynamic switching between two different gamma curves. The CS801-B-I supports virtually unlimited write operations to the on-chip nonvolatile memory.

The CS801-B-I provides gamma and VCOM voltages for an LCD panel potentially replacing discrete components. The CS801-B-I has an I^2C interface for programming both the I^2C registers and EEPROM memory.

With the EEPROM memory and the I^2C interface, the CS801-B-I enables automatic gamma and automatic flicker calibration on a panel-by-panel basis on the production line.

Gamma Buffers

The source drivers can kick back a great deal of current to the buffer outputs during a horizontal line change or a polarity switch. The Gamma Buffer outputs can source/sink 200 mA of peak current to reduce output voltage recovery time when critical levels and patterns are displayed.

VCOM Amplifier

The operational amplifier attached to the VCOM DAC holds the VCOM voltage stable while providing the ability to source and sink 400mA of peak current into the backplane of a TFT-LCD panel. The operational amplifier can directly drive the capacitive load of the TFT-LCD backplane without the need for a series resistor in most cases.

Programmable Reference

The CS801-B-I has an internal 10-bit programmable reference referred to the output. The reference voltage is calculated using the following equation:

$$VREF = (20V \times REF\_CODE)/1024$$

where REF_CODE is the numeric value of the DAC's binary input code and N is the bits of resolution. For the CS801-B-I N = 10 and REF_CODE ranges from 0 to 1023.

10-Bit DACs

VREF sets the full-scale output of the DACs. The Gamma voltage calculation is:

$$VGMA = (VREF \times GMA\_CODE)/1024.$$

The VCOM voltage calculation is:

$$VCOM = (VREF \times VCOM\_CODE)/1024$$

where CODE is the numeric value of the DAC's binary input code stored in registers 0x00 – 0x07 for the gamma outputs and 0x12 for the VCOM output, and N is the bits of resolution. For the CS801-B-I, N = 10 and CODE ranges from 0 to 1023.

The DAC can never output VREF because the maximum value of CODE is always one LSB less than the reference.

Thermal Shutdown

The CS801-B-I features thermal-shutdown protection with temperature hysteresis. When the

die temperature reaches +160°C, the VCOM output and all of the gamma outputs are disabled. When the die cools down by 15°C, the outputs are enabled again.

I²C Serial Interface

The CS801-B-I features an I²C-compatible, 2-wire serial interface consisting of a serial-data line (SDA) and a serial-clock line (SCL). SDA and SCL facilitate communication between the CS801-B-I and the master at clock rates up to 400 KHz. Figure 1 shows the 2-wire interface timing diagram. The master generates SCL and initiates data transfer on the bus. A master device writes data to the CS801-B-I by transmitting the proper slave address followed by the register address and then the data word. Each transmit sequence is framed by a START (S) or REPEATED START (Sr) condition and a STOP (P) condition. Each byte is serially transmitted to the CS801-B-I as 8 bits and is followed by an acknowledge clock pulse. A master reading data from the CS801-B-I transmits the proper slave address followed by a series of nine SCL pulses. The CS801-B-I transmits data on SDA in sync with the master-generated SCL pulses. The master acknowledges receipt of each byte of data. Each read sequence starts with a START (S) or REPEATED START (Sr) condition, and ends with a not acknowledge and a STOP (P) condition. SDA operates as both an input and an open-drain output. A pull up resistor, typically greater than 500Ω, is required on the SDA bus. SCL operates only as an input. A pull up resistor, typically greater than 500Ω is required on the SCL if there are multiple masters on the bus, or if the master in a single-master system has an open-drain SCL output. Series resistors in line with SDA and SCL are optional. Series resistors protect the digital inputs of the CS801-B-I from high-voltage spikes on the bus lines, and minimize crosstalk and undershoot of the bus signals.

Bit Transfer

One data bit is transferred during each SCL cycle. The data on SDA must remain stable during the high period of the SCL pulse. Changes in SDA while SCL is high are control signals (see the START and STOP Conditions section). SDA and SCL idle high when the I²C bus is not busy.

START and STOP Conditions

SDA and SCL are high when the bus is not in use. A master initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA while SCL is high (Figure 2). A START condition from the master signals the beginning of a transmission to the CS801-B-I. The master terminates transmission, and frees the bus by issuing a STOP condition. The bus remains active if a REPEATED START condition is generated instead of a STOP condition.

Early STOP Conditions

The CS801-B-I recognizes a STOP condition at any point during data transmission except if the STOP condition occurs in the same high pulse as a START condition. For proper operation, do not send a STOP condition during the same SCL high pulse as the START condition.

Slave Address

The slave address is defined as the 7 most significant bits (MSBs) followed by the read/write (R/W) bit. Set the R/W bit to 1 to configure the CS801-B-I to read mode. Set the R/W bit to 0 to configure the CS801-B-I to write mode. The address is the first byte of information sent to the CS801-B-I after the START condition. The CS801-B-I slave address is configured with A0. Table 1 shows the possible addresses for the CS801-B-I.

Acknowledge

The acknowledge bit (ACK) is a clocked 9th bit that the CS801-B-I uses to handshake receipt of each byte of data when in write mode (see Figure 3). The CS801-B-I pulls down SDA during the entire master-generated ninth clock pulse if the previous byte is successfully received. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master may retry communication. The master pulls down SDA during the ninth clock cycle to acknowledge receipt of data when the CS801-B-I is in read mode. An acknowledge is sent by the master after each read byte to allow data transfer to continue. A not acknowledge is sent when the master reads the final byte of data from the CS801-B-I, followed by a STOP condition.

Write Data Format

A write to the CS801-B-I consists of transmitting a START condition, the slave address with the R/W

bit set to 0, one byte of data to configure the internal register address pointer, one word (two bytes) or more, and a STOP condition. Figure 4 illustrates the proper frame format for writing one word of data to the CS801-B-I. Figure 5 illustrates the frame format for writing n-bytes of data to the CS801-B-I.

The slave address with the R/W bit set to 0 indicates that the master intends to write data to the CS801-B-I. The CS801-B-I acknowledges receipt of the address byte during the master-generated ninth SCL pulse.

The second byte transmitted from the master configures the CS801-B-I's internal register address pointer. The CS801-B-I's internal address pointer consists of the six least significant bits (LSB) of the second byte. The two MSBs of the second byte (M1 and M0) are set to 00b when writing to the internal registers. See the Memory section for more details. The pointer tells the CS801-B-I where to write the next byte of data. An acknowledge pulse is sent by the CS801-B-I upon receipt of the address pointer data.

The third and fourth bytes sent to the CS801-B-I contain the data that is written to the chosen register and which type of register it writes to either volatile (DAC) or nonvolatile memory (EEPROM). See the Register Address section for more details. An acknowledge pulse from the CS801-B-I signals receipt of each data byte. The address pointer auto increments to the next register address after receiving every other data byte. This auto increment feature allows a master to write to sequential register address locations within one continuous frame. The master signals the end of transmission by issuing a STOP condition.

Read Data Format

The master presets the address pointer first by sending the CS801-B-I's slave address with the R/W bit set to 0 followed by the register address with M1 and M0 set to 00b after a START condition. The CS801-B-I acknowledges receipt of its slave address and the register address by pulling SDA low during the ninth SCL clock pulse. A REPEATED START condition is then sent followed by the slave address with the R/W bit set to 1. The CS801-B-I transmits the contents of the specified register. Transmitted data is valid on the rising edge of the master-generated serial clock (SCL). The address pointer auto increments after every other read data byte. This auto increment feature allows all registers to be read sequentially within one continuous frame. A STOP condition can be issued after any number of read data bytes. An attempt to read from a reserved register address results in repeated reads from a dummy register containing data of all zeros. The master acknowledges receipt of each read byte during the acknowledge clock pulse. The master must acknowledge all correctly received bytes except the last byte. The final byte must be followed by a not acknowledge from the master and then a STOP condition. Figures 6 and 7 illustrate the frame format for reading data from the CS801-B-I.

Registers

Register Map

The CS801-B-I has two banks of nonvolatile EEPROM memory and a bank of volatile memory comprised of I^2C registers and DAC registers. Each memory location, whether in nonvolatile or volatile memory, holds a 10-bit word. Two bytes must be read or written through the I^2C interface for every access. Table 2 shows the register map. The write control bits determine which memory location the data is stored into.

Register Description

Only the 10 least significant bits (LSBs) are written to the GAMMA and VCOM registers (see Table 3). During a write operation, the write control bits (the two MSBs) are stripped from the incoming data stream and are used to determine whether the EEPROM or DAC registers are updated (see Table 4).

The write control bits W1 and W0 control whether it is the DAC latches or the selected EEPROM bank registers that get written to. The EEPROM bank is selected by the BKSEL pin.

VCOM Programmable Range

The CS801-B-I features programmable range for VCOM. VCOMMIN and VCOMMAX registers provide low and high limits for the VCOM DAC register. At the factory, VCOMMIN is set to 0 and VCOMMAX is set to 1023 (default values) to provide the full programmable range for VCOM. Later, the user can define the limits by programming VCOMMIN and VCOMMAX registers and the EEPROM.

The 0x1E of VCOM MAX calculation is:

VCOMMAX= (VREF x VCOM_CODE)/1024

The 0x1E VCOM MAX register can restrict VCOM register output values, when the VCOM setting output is higher than that of VCOM MAX output, the output of VCOM will be restricted on the VCOM MAX value.

The 0x1F of VCOM MIN calculation is:

VCOMMIN= (VREF x VCOM_CODE)/1024

The 0x1F VCOM MIN register can restrict VCOM register output values, when the VCOM setting output is lower than that of VCOM MIN output, the output of VCOM will be restricted on the VCOM MIN value.

VCOM register values are limited to the defined range. This means if the VCOM register accidentally gets programmed with a value higher than VCOMMAX, it automatically gets locked to the VCOMMAX value. The I^2C bus does acknowledge and receive the data sent on the bus, however, internally the part recognizes that the value is outside of the range and adjusts it accordingly. The same scenario is true if the value programming VCOM is below VCOMMIN.

Memory

The CS801-B-I includes both volatile memory for the I^2C and DAC registers and 2 banks of nonvolatile memory (EEPROM). It is possible to write to each single DAC and I^2C memory location from an EEPROM memory location individually or to write to them all at once. This is done with memory write bits (M1, M0) that are the two MSBs of the register address byte. Table 5 shows the memory write bits. Set both M1 and M0 to low or high when writing to or reading from the register values through I^2C bus.

Volatile Memory

The CS801-B-I features a double-buffered register structure. The volatile (DAC) memory can be updated without updating the output voltage. Figure 8 shows how to program a single DAC. The output voltage is updated after sending LSB (D0),

It is possible to write to multiple DACs first then update the output voltage of all channels simultaneously, as shown in Figure 9. In this mode, it is possible for the I^2C master to write to all registers of the CS801-B-I (Gamma and VCOM) in one communication. In that case, the values programmed in reserved addresses are meaningless. However, the CS801-B-I does send an acknowledge bit for each of the two bytes on any of these addresses. The control bits (M1, M0) shown in Figure 6 are set in a way that all DACs are programmed to their desired value with no changes to the output voltages until the LSB of the last DAC is received; then all the channels update simultaneously.

Nonvolatile Memory

The CS801-B-I is able to write to either bank, selected by the BKSEL pin, of nonvolatile memory (EEPROM) of any single DAC/VCOM register in a single or burst I^2C transaction. This memory can be written to at least 10,000 times. Figure 10 shows a single write to an EEPROM address. The control bits in Figure 10 are set in a way that the EEPROM register is updated at the end of LSB (D0).

Figure 11 shows how to program multiple EEPROM registers in one communication transition. Similar to programming the volatile memory, the first 2 bytes of data corresponds to the DAC/VCOM address specified by the master on the previous byte and the following 2 bytes of data correspond to the next address and so on. In this configuration all the EEPROM registers are programmed at the same time following the LSB of the last set of data bytes. (The last set of data bytes is different than the previous bytes as its bit 15 and bit 14.) If for some reason the master issues a stop condition before sending last two bytes of the data with appropriate values of bit 15 and bit 14 (01) then none of the EEPROM registers are updated.

Programming the EEPROM registers also updates the DACs/VCOM volatile memory as well as the output voltages. Similar to multiple volatile memory programming, the update only occurs after the EEPROM memory is programmed. During EEPROM program time, the CS801-B-I is not available on the I^2C and any communication from the master should be delayed until the EEPROM is programmed. Any attempt from the I^2C master to talk to the CS801-B-I is not acknowledged.

General and Single Acquire Commands

It is possible to update all of the DAC outputs to the previously stored EEPROM values from either selected EEPROM bank with one special command. Set the 2 MSB bits (M1 and M0) of the DAC/VCOM address to 10 to set all the DACs and the output voltages to the values of EEPROM (as shown in Figure 12). The CS801-B-I ignores the DAC/VCOM address in this case. Toggling the BK_SEL pin will change all nine programmable

buffer outputs to the gamma correction curve stored in the selected bank at the same time after a 750us delay.

It is also possible to update the DAC and output voltage of only one channel from the EEPROM. Set the 2 MSB bits (M1 and M0) of the DAC/VCOM address to 01 (as shown in Figure 13) to move a specific value from EEPROM into the DAC and output voltage of a single channel.

The CS801-B-I features a double-buffered register structure. It is important to note that updating the volatile (DAC) memory is not the same as updating the output voltage. It is possible to write to multiple DACs first then update the output voltage of all channels simultaneously in one of two ways:

In the first way, the master sets data bit 15 to '1' for each write transaction, and then the DAC/VCOM voltage is updated after the 16th data bit for the currently written word is received. This is useful for changing the DAC/VCOM voltages immediately after writing to a DAC register.

In the second way, the master writes to the desired DAC/VCOM channels with bit 15 set to '0'. Then the master sets bit 15 to '1' when writing the last desired DAC/VCOM channel. When the 16th data bit is received, all DAC/VCOM channels are updated.

VCOM Operational Amplifier Programmable Gain

The VCOM gain can be adjusted by programming the values in the VCOM gain register through the I^2C interface. -6V/V in -1V/V steps can be programmed through the I^2C register adjustable integrated gain and feedback resistors incorporated in the VCOM operational amplifier. VCOM can also be programmed as a unity gain buffer (+1V/V), or can be programmed to set its gain with external resistors.

Power-Up and Power-Down

The digital supply must be powered up before Analog supply. For power-down, Analog supply must be powered down first and then digital supply can safely be powered down.

Power UP and General-Call Reset Function

At power up CS801-B-I resets and reads the internal non volatile memory and all the outputs are set corresponding to the last programmed non-volatile memory values.

The General Call Reset function is an I^2C command that has special address byte of 00h followed by data byte 06h. Refer to figure 14. When the CS801-B-I receives this command, then, like power on reset, all the outputs are set to the values corresponding to the last programmed non-volatile memory data.

Power Supplies and Bypass Capacitors

The CS801-B-I operates from a single 9V to 20V analog supply (AVDD) and a 2.7V to 3.6V digital supply (DVDD). Bypass AVDD to GND with 0.1uF and 10uF capacitors in parallel. Use an extensive ground plane to ensure optimum performance. Bypass DVDD to GND with a 0.1uF capacitor. The 0.1uF bypass capacitors should be as close as possible to the device.

Layout and Grounding Exposed Pad

If the CS801-B-I is mounted using reflow soldering or wave soldering, the ground via(s) for the exposed pad should have a finished hole size of at least 14 mils to insure adequate wicking of soldering onto the exposed pad. If the CS801-B-I is mounted using a solder mask technique, the via requirement does not apply.

In either case, the exposed pad must be connected to both digital and analog grounds through a low thermal resistance path to ensure adequate heat dissipation. Do not route traces under the package.

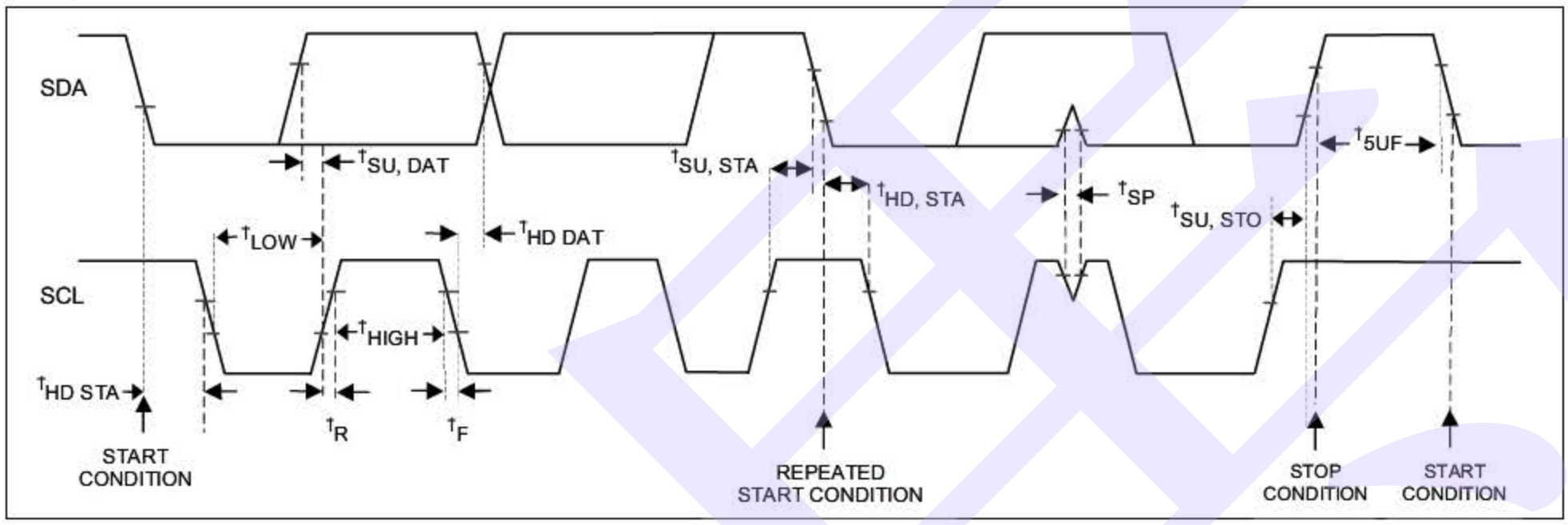


Figure 1. I^2C Serial- Interface Timing Diagram SMBus is a trademark of Intel Corp.

Table 1 Slave Address

A1	A0	READ ADDRESS	WRITE ADDRESS
DGND	DGND	E9h	E8h
DGND	DVDD	EBh	EAh
DVDD	DGND	EDh	ECh
DVDD	DVDD	EFh	EEh

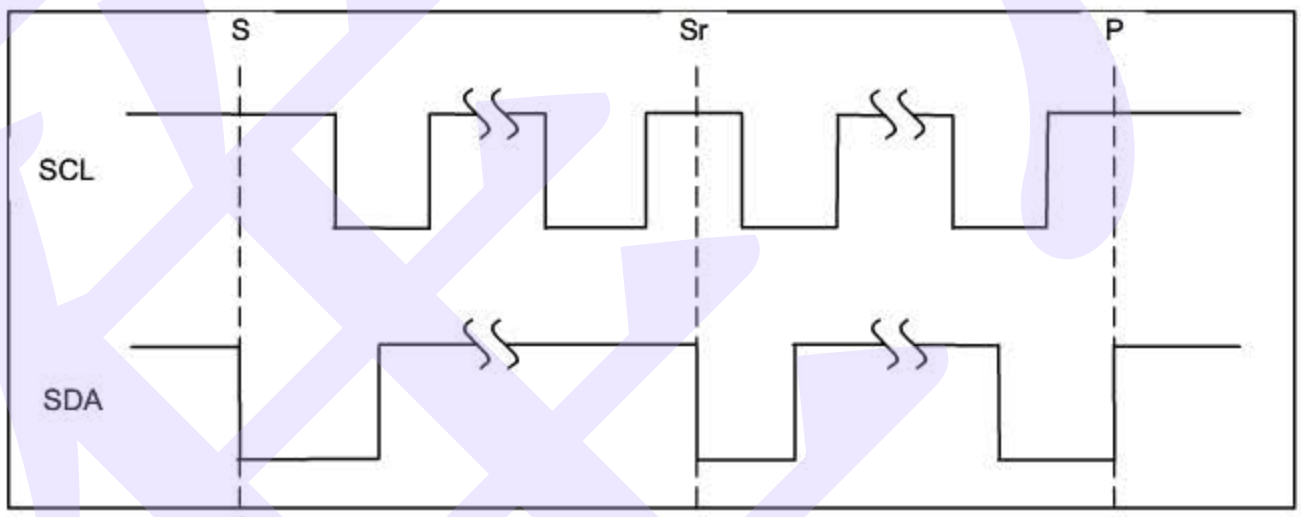


Figure 2. START, STOP and REPEATED START Conditions

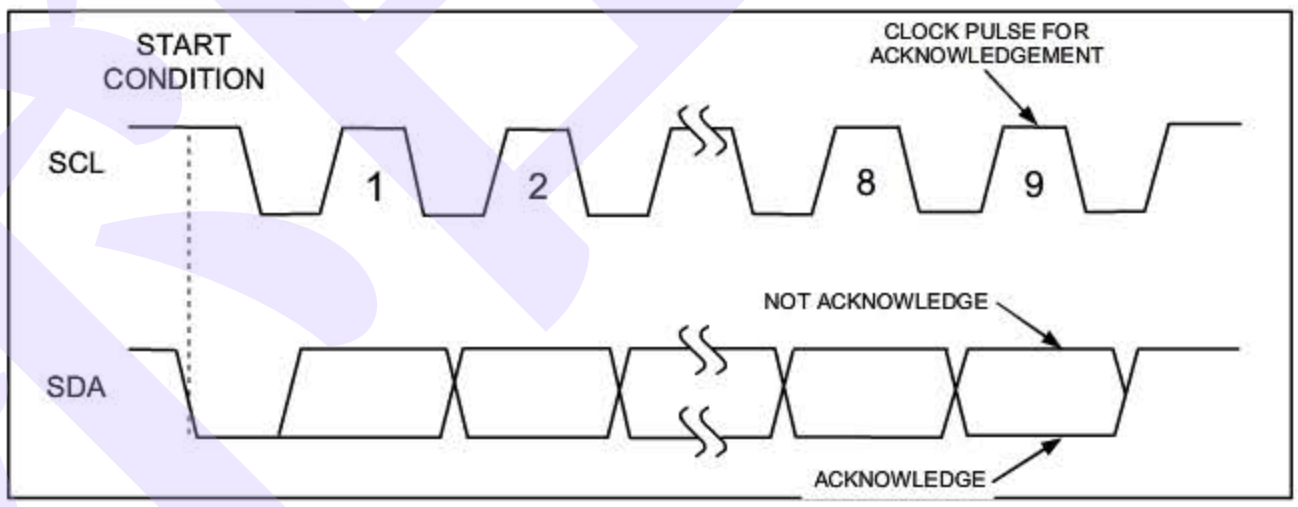


Figure 3. Acknowledge

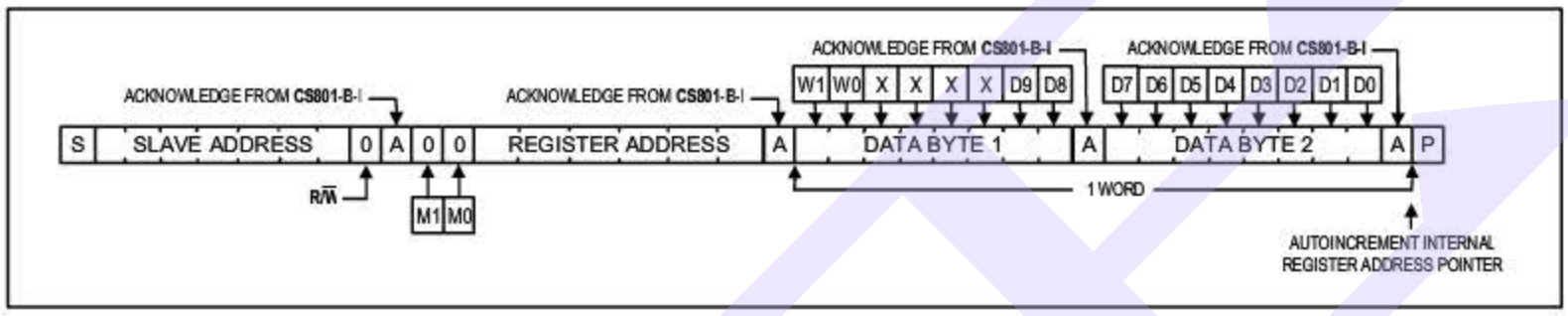


Figure 4. Writing a Word of Data to the CS801-B-I

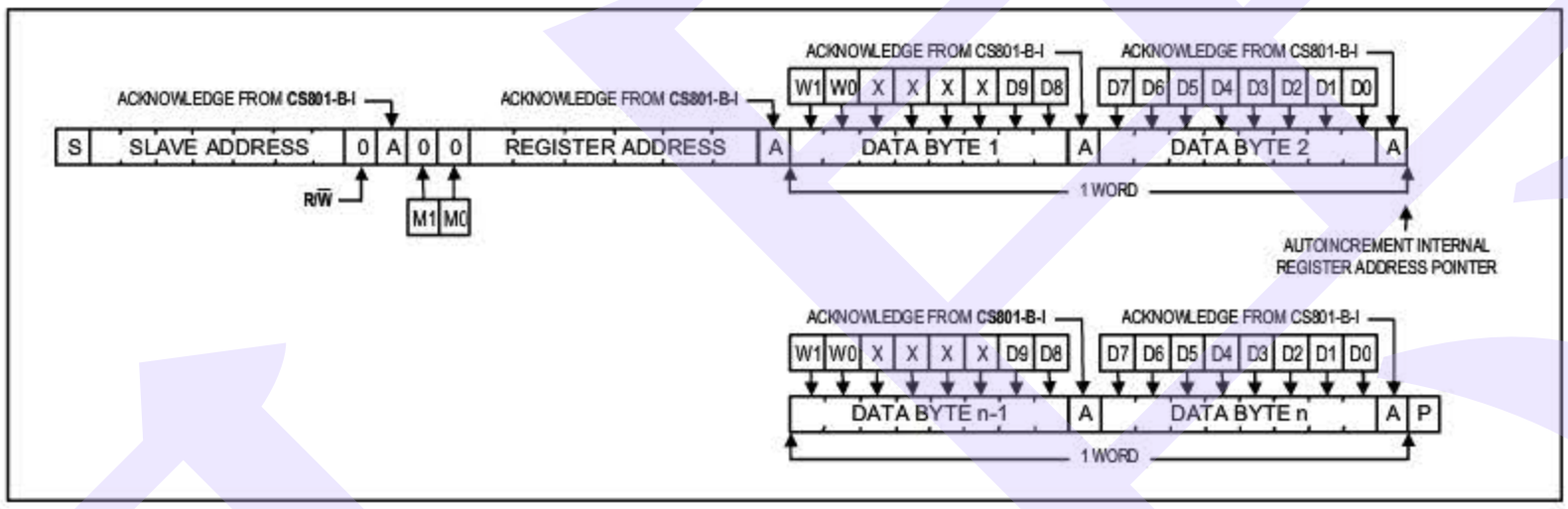


Figure 5. Writing n Bytes of Data to the CS801-B-I

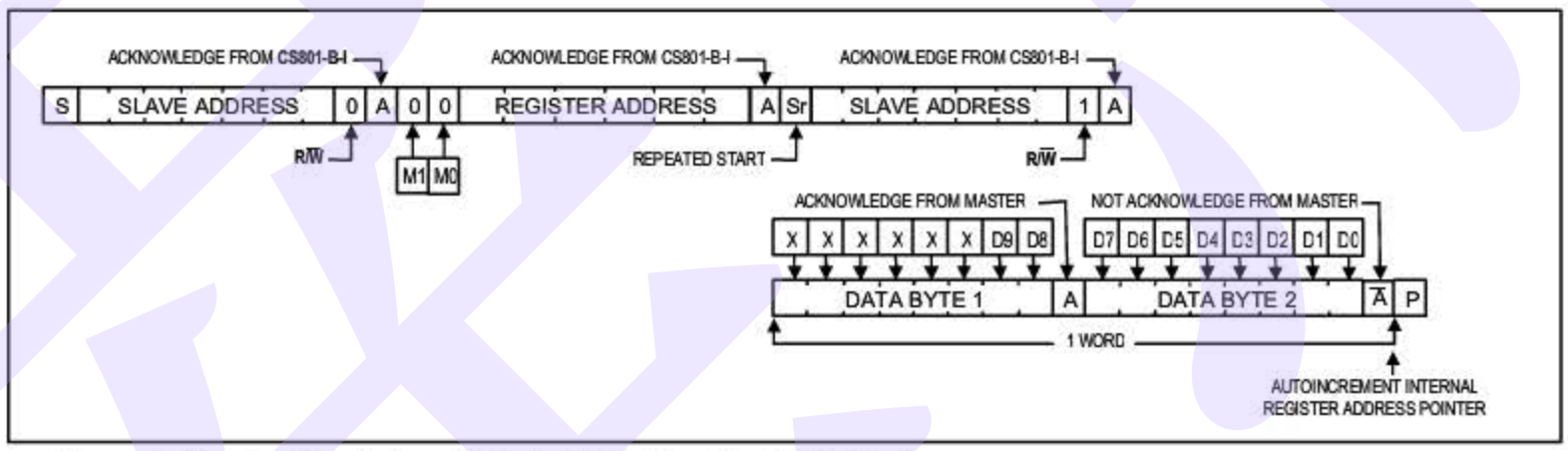


*Figure 6. Reading One Indexed Word of Data from the **CS801-B-I***

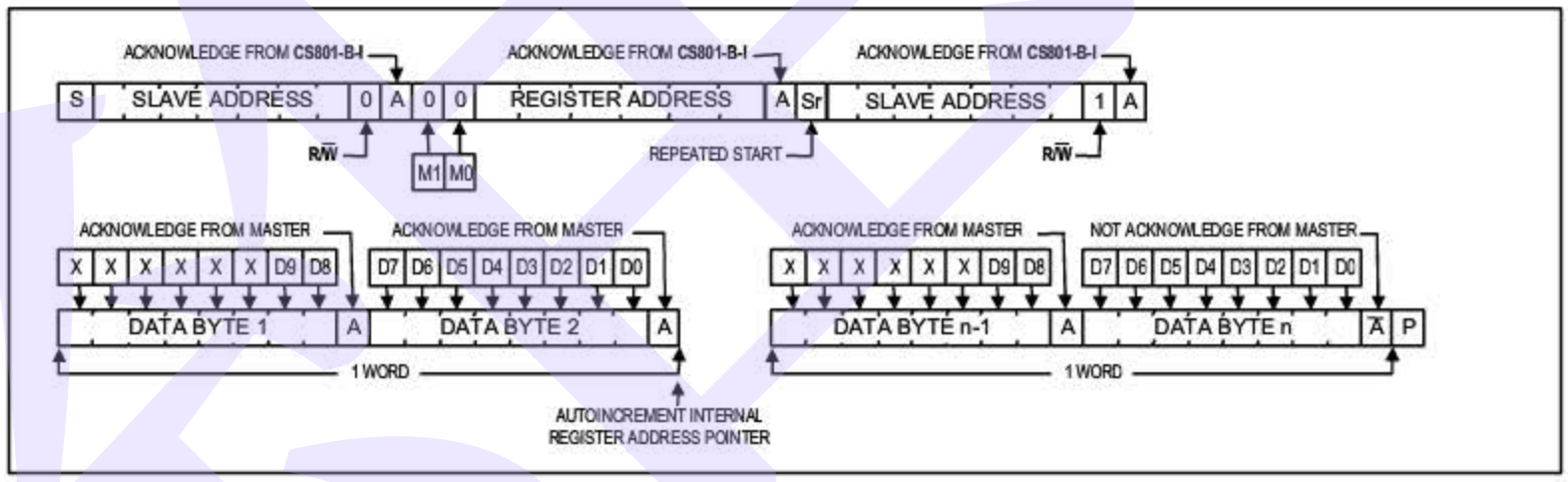


*Figure 7. Reading n Bytes of Indexed Data from the **CS801-B-I***

Table 2. Register Map

REGISTER ADDRESS in HEX	REGISTER NAME	REGISTER DESCRIPTION	MTP FACTORY INITIALIZATION VALUE	READ/WRITE?
0x00	GMA 1	Gamma 1	0x3FF	Read and write
0x01	GMA 2	Gamma 2	0x200	Read and write
0x02	GMA 3	Gamma 3	0x200	Read and write
0x03	GMA 4	Gamma 4	0x200	Read and write
0x04	GMA 5	Gamma 5	0x200	Read and write
0x05	GMA 6	Gamma 6	0x200	Read and write
0x06	GMA 7	Gamma 7	0x200	Read and write
0x07	GMA 8	Gamma 8	0x200	Read and write
0x08	VREF	Internal Reference	0x2D7	Read and write
Reserved address range				
0x12	VCOM	Common Voltage	0x200	Read and write
Reserved address range				
0x1C	VCOM GAIN SET	Gain set register	0x0000	Read and write
0x1E	VCOM MAX	Maximum VCOM value	0x3FF	Read and write
0x1F	VCOM MIN	Minimum VCOM value	0x000	Read and write
Reserved address range				
0x3C	Die Rev	Die Revision	NA	Read Only (0x0000 first Rev)
0x3D	Die ID	Die ID	NA	Read Only (0x0000 First Die)
0x3E	Memory raw data	Memory Raw data	NA	Read Only (0x0000 always)
0x3F	MAXBANK	-	NA	Read Only (0x0000 always)

Note: All the registers are 2 byte (16 bits) with valid lower significant bits out of 16bits as applicable to individual registers.

For example

1) **VCOM GAIN SET REGISTER 2 BYTE FORMAT IS ---- X X X X X X X X B7 B6 B5 B4 B3 B2 B1 B0 (16 bit)**
2) **GAMMA & VCOM registers 2 BYTE FORMAT IS ---- X X X X X X B9 B8 B7 B6 B5 B4 B3 B2 B1 B0 (16 bit)**
3) **All channel read and write will be in 2 byte (16bit) format with valid lower bits.**

Table 3. Register Description

REG	REF ADDR	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
GMA1	0x00	W1	W0	X	X	X	X	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
GMA2	0x01	W1	W0	X	X	X	X	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
GMA3	0x02	W1	W0	X	X	X	X	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
GMA4	0x03	W1	W0	X	X	X	X	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
GMA5	0x04	W1	W0	X	X	X	X	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
GMA6	0x05	W1	W0	X	X	X	X	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
GMA7	0x06	W1	W0	X	X	X	X	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
GMA8	0x07	W1	W0	X	X	X	X	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
VREF	0x08	Note: See Fig. 15,16		X	X	X	X	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Reserved	0x09	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
RESERVED ADDRESS RANGE WHEN READ WILL ALWAYS READ 00 FOR RESERVED ADDRESSES																	
VCOM	0x12	W1	W0	X	X	X	X	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
RESERVED ADDRESS RANGE WHEN READ WILL ALWAYS READ 00 FOR RESERVED ADDRESSES																	
GAIN SET	0X1C	W1	W0	X	X	X	X	X	X	b7	b6	b5	b4	b3	b2	b1	b0
VCOMMAX	0x1E	W1	W0	X	X	X	X	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
VCOMMIN	0x1F	W1	W0	X	X	X	X	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
RESERVED ADDRESS RANGE WHEN READ WILL ALWAYS READ 00 FOR RESERVED ADDRESSES																	
Die Rev	0x3C	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Die ID	0x3D	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Mem raw data	0x3E	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
MAXBANK	0x3F	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
RESERVED ADDRESS RANGE WHEN READ WILL ALWAYS READ 00 FOR RESERVED ADDRESSES																	

Table 4. Write Control Bits

W1	W0	ACTION
0	0	No update.
0	1	All EEPROM registers get updated when the current I^2C register has finished updating (end of B0).
1	0	All DAC registers get updated when the current I^2C register has finished updating (end of B0).
1	1	No update.

Table 5. Memory Write Bits

M1	M0	ACTION
0	0	None.
0	1	Only the addressed I^2C registers DAC registers get set to the EEPROM values.
1	0	All I^2C registers and DAC registers get set to the EEPROM values.
1	1	None.

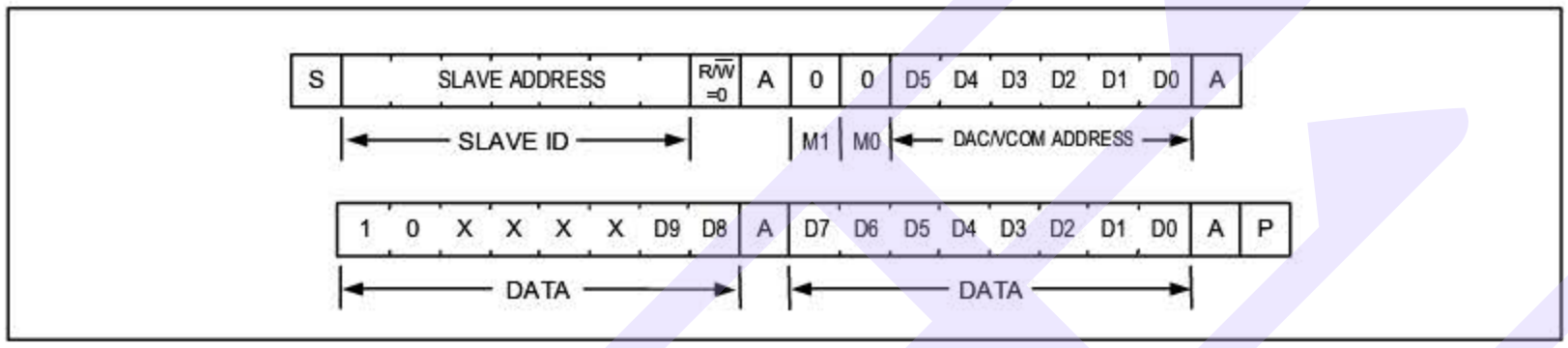


Figure 8. Single DAC Programming

Figure 9. Multiple DAC Programming

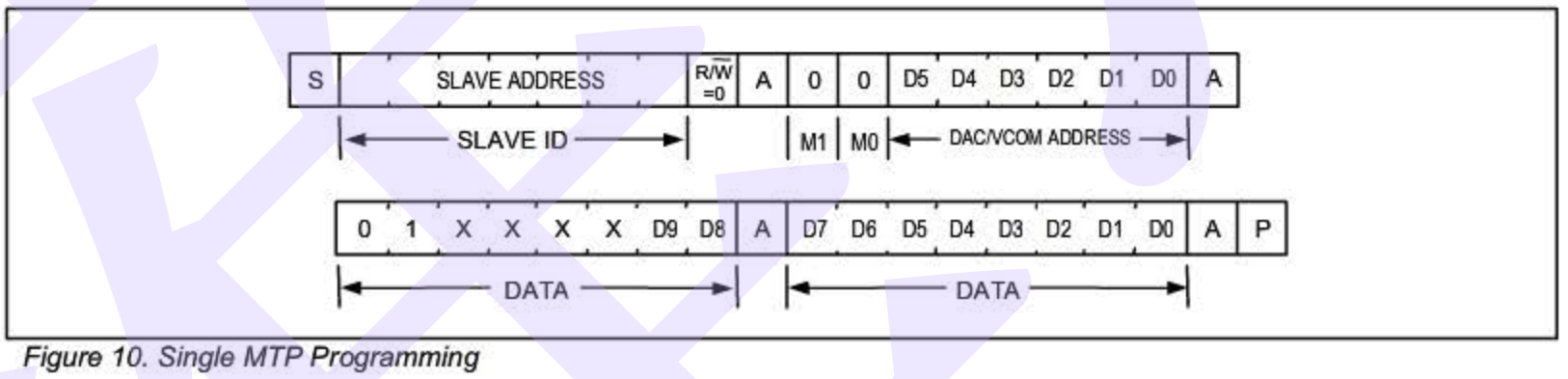


Figure 10. Single MTP Programming

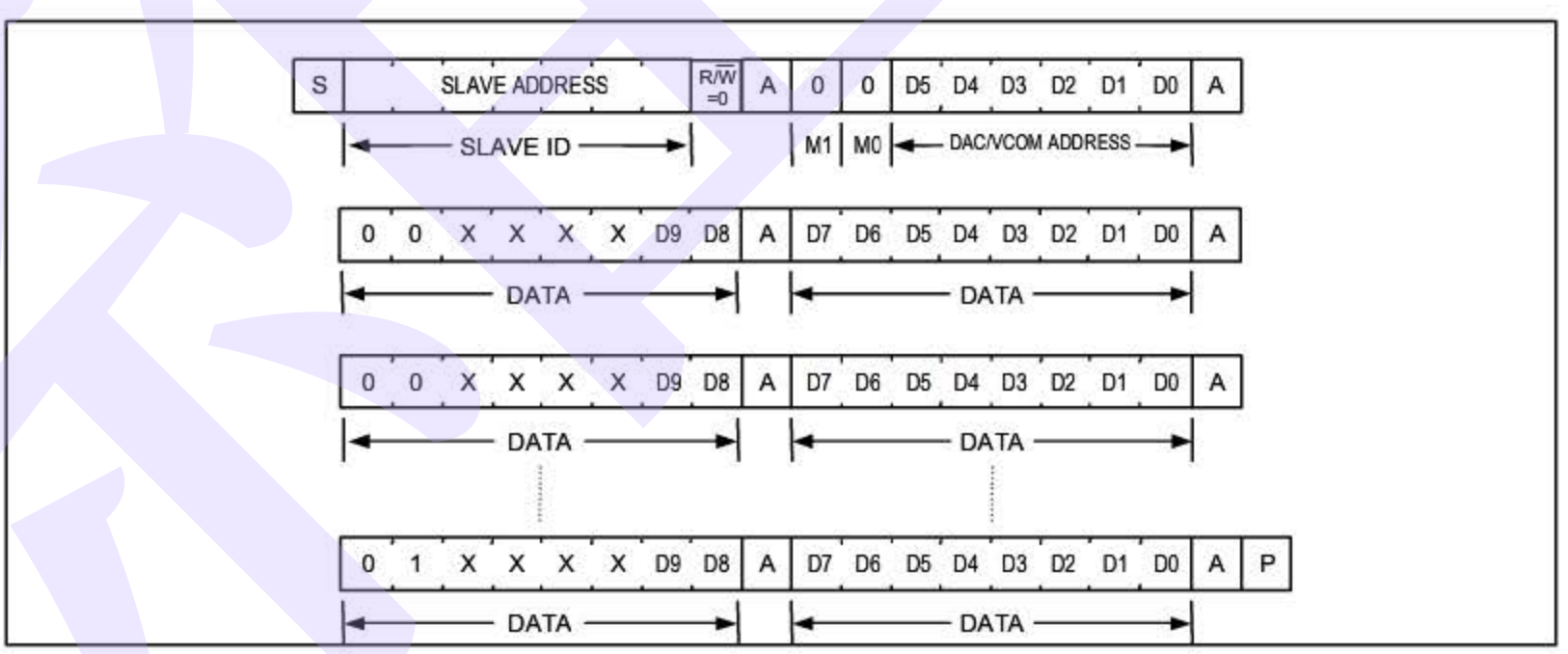


Figure 11. Multiple MTP Programming

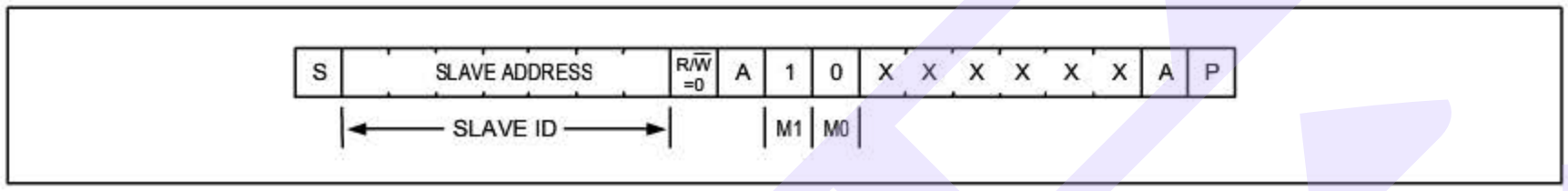


Figure 12. General Acquire Command to Update All Outputs with EEPROM

Figure 13. Single Acquire Command to Update One Output with MTP

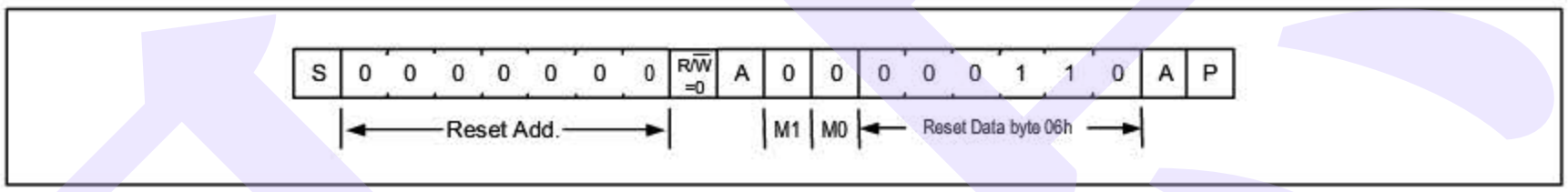


Figure 14. General Call Reset Function

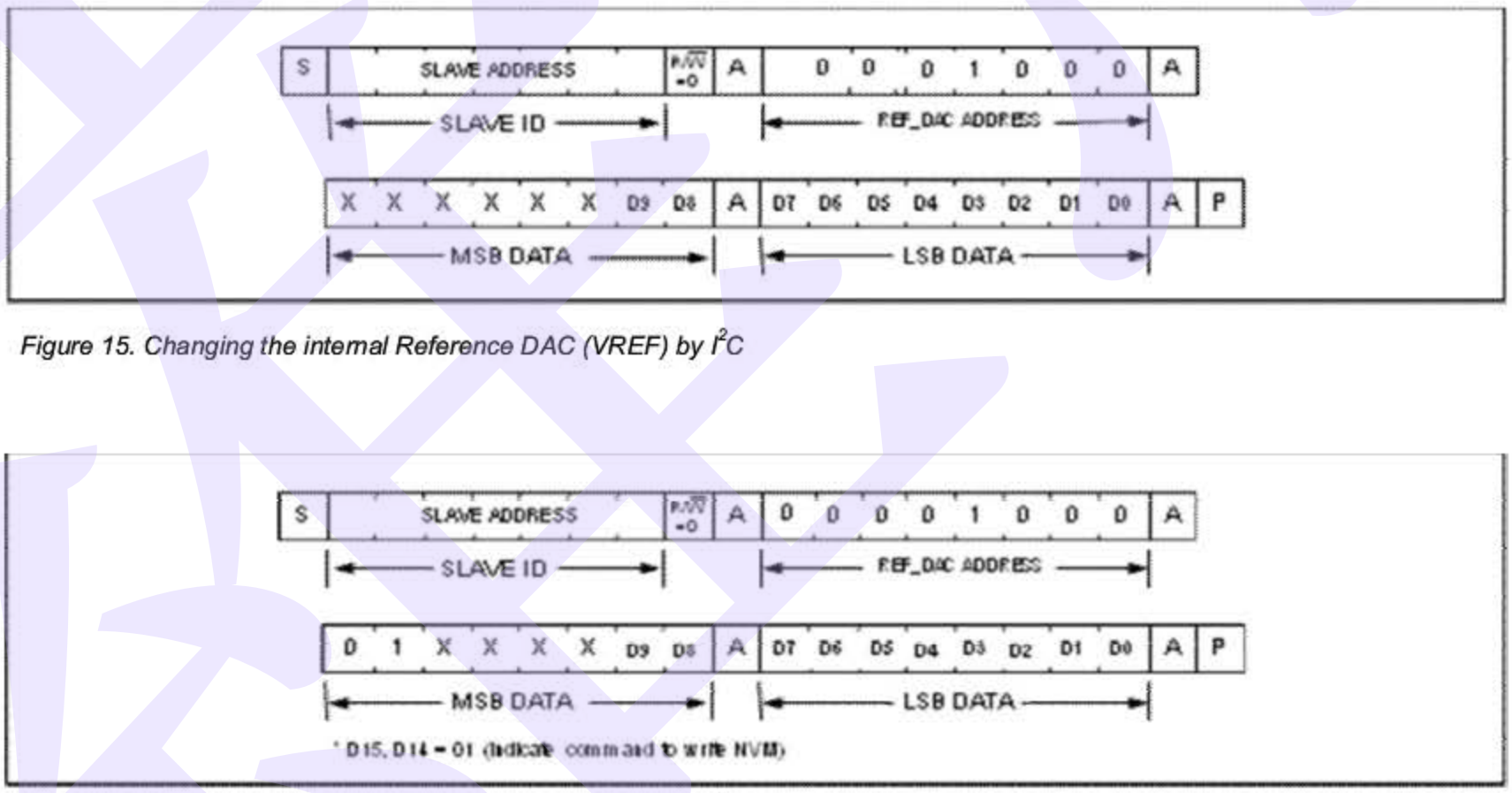
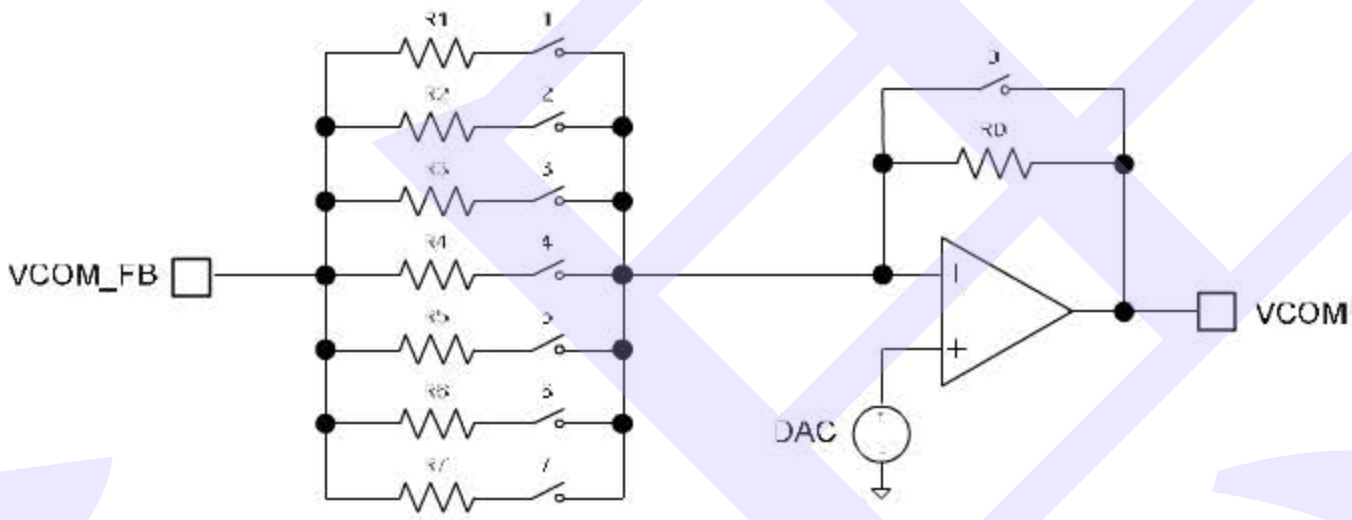


Figure 15. Changing the internal Reference DAC (VREF) by I^2C

Figure 16. Changing the internal Reference DAC (VREF) by I^2C and Writing Data to NVM

Adjustable VCOM Gain

Vcom has 8 internal adjustable gain configurations that are selected by user through the I²C bus. Selectable gains include the buffer gains of 1, 2, 3, 4, 5 and 6 for switch positions 1, 2, 3, 4, 5, and 7.
Table 7 depicts the approximate values (±15%) of the internal resistors in the feedback configuration in the below figure.



Configuration for switch positions

Table 6 VCOM Gain Set Register.

Reg Name	Reg Address	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
VCOM Gain	1C	W1	W0	X	X	X	X	X	X	E	6	5	4	3	2	1	U

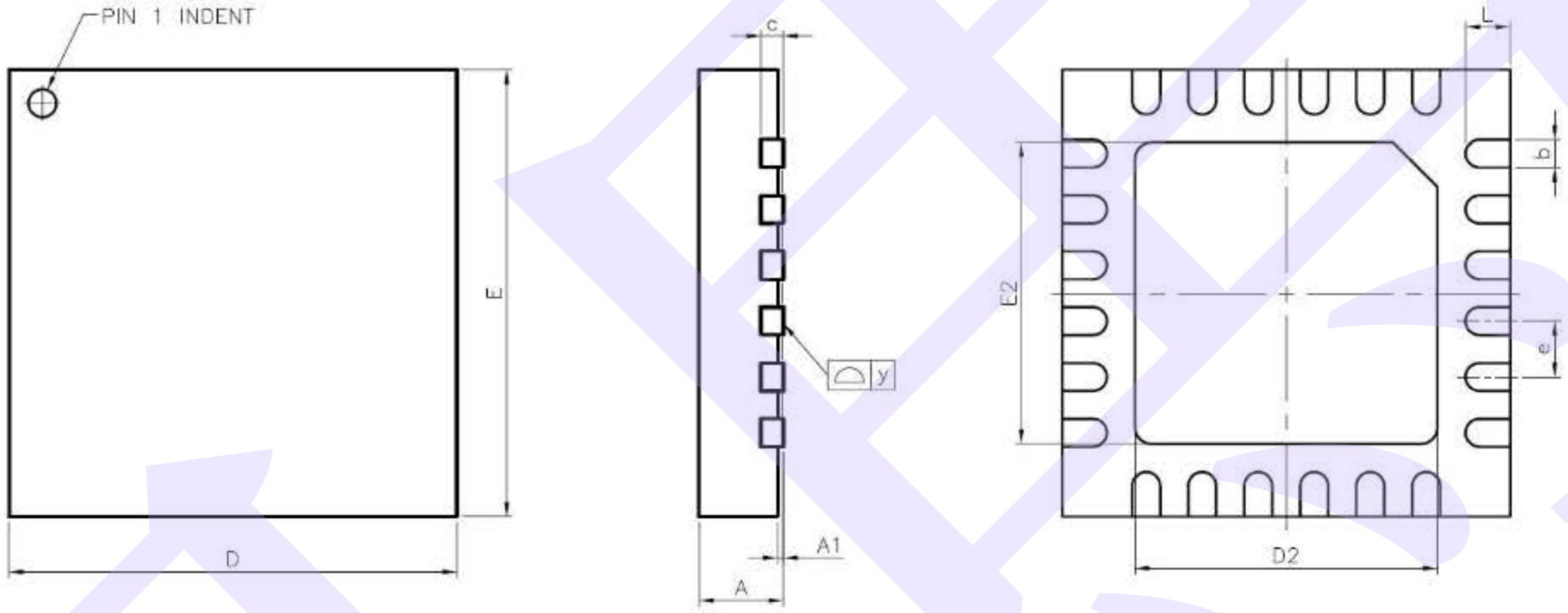
Table 7 VCOM Gain Configuration.

Switch Position	Value	Gain	Reg[7:0]	Control Mode
0	R0 = 78K	1	00000001	Unity Gain
1	R1 = 78K	R0 / R1 = 1	00000010	Internal Gain
2	R2 = 39K	R0 / R2 = 2	00000100	
3	R3 = 26K	R0 / R3 = 3	00001000	
4	R4 = 19.5K	R0 / R4 = 4	00010000	
5	R5 = 15.6K	R0 / R5 = 5	00100000	
6	R6 = 13K	R0 / R6 = 6	01000000	
7	R7 = 6.5K	R0 / (R7 + REX)[1]	10000000	External Gain

Note: 1. The external resistor (REX) can be set up to 70KΩ

Package Information

24 Pin TQFN (4x4)



Note: The terminal #1 identifier is a laser marked feature

SYMBOLS	DIMENSIONS IN MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
c	——	0.20 REF.	——
D	3.95	4.00	4.05
D2	2.65	2.70	2.75
E	3.95	4.00	4.05
E2	2.65	2.70	2.75
e	——	0.50	——
L	0.35	0.40	0.45
y	0.00	——	0.075