Data Sheet

BIT3501

High Performance PWM Controller

Version: A4

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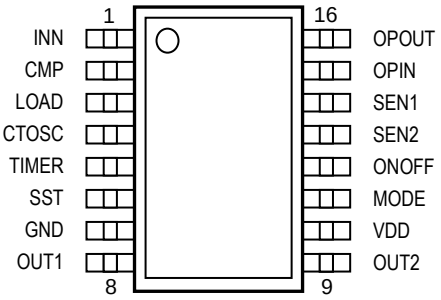
Features:

- **3.1V ~ 5.5V operation**
- **Fixed High Frequency, Voltage Mode PWM Control Topology**
- **Latched Off Protection**
- **Programmable Soft Start**
- **Build-In UVLO**
- **Low Power CMOS Process**
- **Selectable Totem Pole Output**
- **16 Pin Package**

Pin Layout:



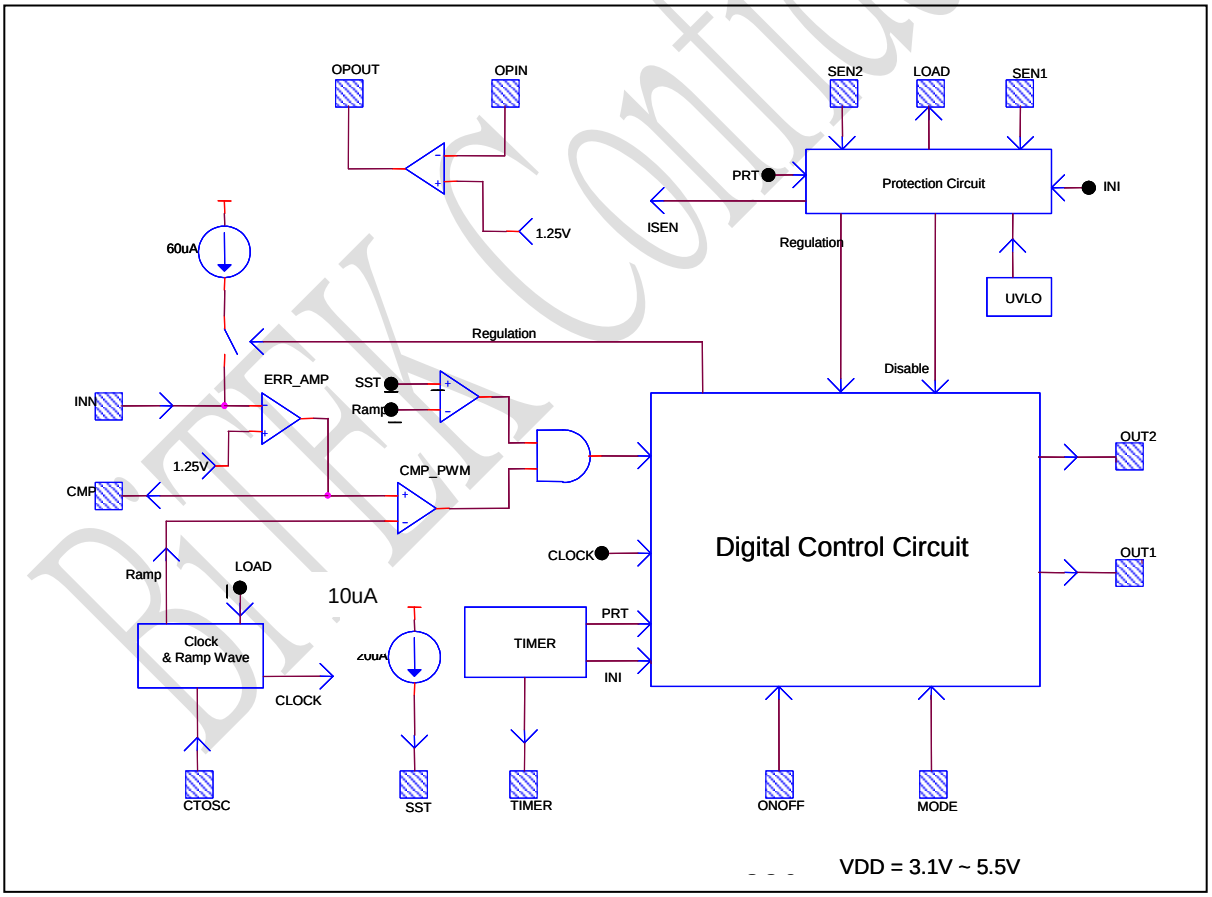
General Description:

BIT3501 provides the essential features for DC/DC conversion PWM controller in a small low cost 16-pin package. BIT3501 includes latched off protection feature may make the system more reliable while compare to other similar products. Selectable outputs provide user more flexibility while facing different applications.

Recommended Operating Condition:

Supply Voltage..... 3.1V ~ 5.5V
Operating Frequency(CTOSC)..... .50K ~ 200K Hz
Operating Ambient Temperature..... -20 ~ 85 ℃

Functional Block Diagram:



Pin Description:

Pin No.	Symbol	I/O	Descriptions
1	INN	I	The inverting input of the error amplifier.
2	CMP	O	Output of the error amplifier.
3	LOAD	I/O	An internal switch is on LOAD pin. During start-up mode, if SEN1<1.3V, the internal switch is closed, an external resistor is connected on LOAD to change the operation frequency of CTOSC. After ISEN>1.3V, the switch is open. During operation, the internal switch is open.
4	CTOSC	I/O	An external capacitor is connected here to set the frequency of the PWM controller.
5	TIMER	I/O	With internal reference current and an external capacitor to set the different operational mode. There are three modes. 1. Reset mode (0V < TIMER <0.3V): The output current of this pin is almost 20uA 2. Start-up mode (0.3V < TIMER < 1.8V): The output current of this pin is almost 1uA. All the protection functions are disabled in this mode. 3. Normal operation mode (TIMER>1.8V): All the protection functions are enabled in this mode. If ISEN is lower than 1.3V or OUTADJ is higher than 2V, OUT1 and OUT2 will be latch-off.
6	SST	I/O	Soft Start output. The output current of this pin is 10uA. With this current to charge a capacitor connected in this pin can set the slope of soft start.
7	GND	I/O	The ground pin of the device.
8	OUT1	O	High active output driver.
9	OUT2	O	Output driver pin. It is “low active” when MODE pin is pulled to VDD and becomes “high active” when MODE pin is pulled to GND.
10	VDD	I	The power supply pin of the device.
11	MODE	O	To set the output polarity of the OUT2. The Mode is “1” while connects to VDD. The Mode is “0” while connects to GND.
12	ONOFF	I	The control pin turns on or turns off chip.
13	SEN2	I	During start-up mode, if SEN2 > 1.5V and 1.8V>TIMER>0.3V, a 60uA current will flow into INN to adjust CMP to regulate the output. if SEN2>1.5V and Timer > 1.8V continue 32 cycles of PWM operation frequency, the circuit is latch-off.
14	SEN1	I	During start-up mode, if SEN1<1.3V, the internal switch on LOAD pin will be closed. If SEN1>1.3V, the switch will be open. During operation mode, if SEN1<1.3V continue 32 cycles of PWM operation frequency, the circuit is latch-off..
15	OPIN	I	The inverting input of the operational amplifier.
16	OPOUT	I/O	The output of the operational amplifier.

Functional Description:

Selectable Output: The polarity of OUT2 is determined by MODE pin. When MODE is connected to GND, OUT2 is "high active". When MODE is connected to VDD, OUT2 is "low active".
OUT1 is always a "high active" output.

CTOSC Frequency Set Up: CTOSC frequency is determined by an external capacitor on CTOSC pin. CTOSC frequency is 100 KHz when an 820pF capacitor is connected to CTOSC. The equation (1) describes the relationship between external capacitor and CTOSC frequency.

$$F_{CTOSC} = \frac{K_{CTOSC}}{C_{CTOSC}},\ K_{CTOSC} = 8.2e-5 \text{.....(1)}$$

Equation (1) is valid only when VDD=5.0V, temperature=40ºC and frequency ≈ 80K ~ 120 KHz. Fig. 3 shows the relationship between CTOSC frequency and external capacitor.

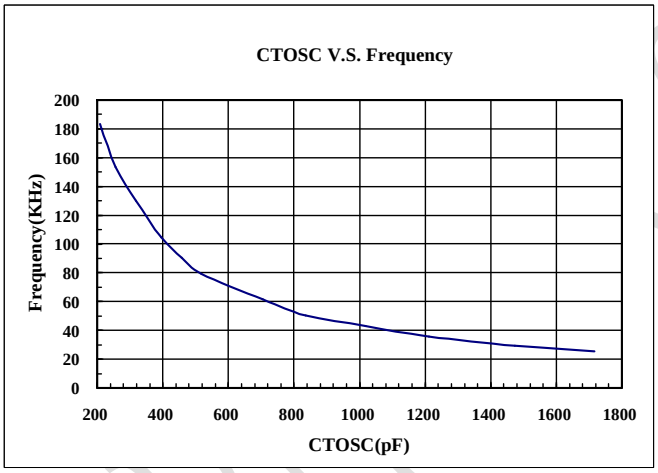


Fig.3

Power On Initialization: An internal current source charges the external capacitor on TIMER pin to determine the initialization timing of BIT3501. This current provides 20uA when TIMER is less than 0.3V, and 1uA when TIMER is larger than 0.3V. The circuit is in reset mode when TIMER is less than 0.3V. Table 2 lists the status of some pins during TIMER less than 0.3V.

Table 2 BIT3501 initial states

Pin	Pin Name	Status
4	CTOSC	Normally free run
6	SST	Forced to GND level
8	OUT1	Forced to GND level
9	OUT2	Forced to GND level (MODE=0)
9	OUT2	Forced to VDD level (MODE=1)

The Programmable Soft Start: A current mirror provides 10uA current to charge the SST. The slope of Soft Start ΔV/ΔT is determined by equation (2).

$$\frac{\Delta V}{\Delta T} = \frac{10uA}{C_{SST}} \text{..... ..(2)}$$

The Latch-off Protection_1: The SEN1 pin may be used to detect the circuit is operated as designed. In most applications, it defines "start-up period" while TIMER <1.8V, no protection function is performed., so that BIT3501 disable the latched off functions. If SEN1 < 1.3V and TIMER > 1.8V after 32 cycles of PWM operation frequency, BIT3501 will shut down OUT1 and OUT2 until the system is powered on or enabled again.

The Latch-off Protection_2: The SEN2 is another control loop to regulate the output while TIMER <1.8V. In this state, a 60uA output current will charge the INN to adjust CMP while SEN2 > 1.5V. SEN2 also provides the latched off protection performs while TIMER > 1.8V.
In this state if TIMER > 1.8 V and SEN2 > 1.5 V after 32 cycles of PWM operation frequency, BIT3501 will shut down OUT1 and OUT2 until the system is powered on or enabled again.

CTOSC Frequency In Different Mode: In many cases, the optimal operation frequency of the circuit is different while the operation conditions change. To obtain the better performance, the operation frequency of the PWM controller must be controlled properly. The LOAD pin is used to change the frequency of CTOSC by external resistor. When Timer < 0.3V, the circuit is in reset mode. When 1.8V > Timer > 0.3V, the circuit is in start-up mode. CTOSC frequency is changed by an external resistor on LOAD pin. The relationship between CTOSC frequency and LOAD resistor is as Fig (4). When timer > 1.8V, the circuit is in normal operation mode. With an 820pF capacitor on CTOSC, CTOSC frequency is 100 KHz.

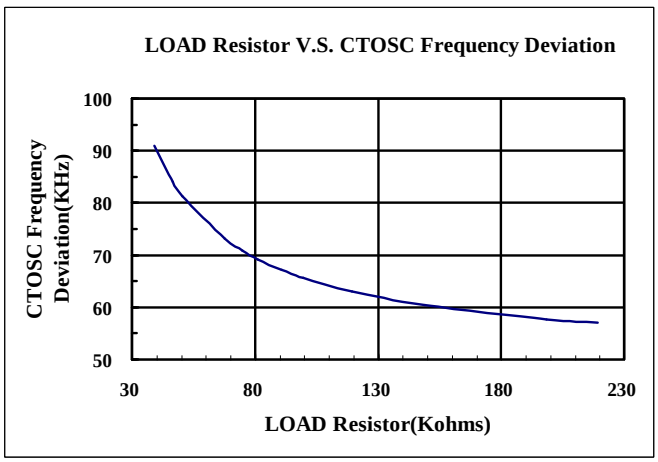


Fig.4

UVLO: The under-voltage-lockout circuit turns off the output driver when supply voltage drops too low. Whole system includes the protection and timing circuits are reset (pin TIMER =0) in low VDD state.

DC/AC Characteristics:

Absolute Ratings:

Table 3

Parameter	Symbol	Ratings	Unit	Remarks
Supply Voltage	VDD	-0.3~+ 6	V	Ta=25°C
Ground	GND	±0.3	V	
Input pin Voltage		-0.3~ VDD+0.3	V	
Operating Ambit Temperature	Ta	0 ~ +85	˚C	
Operating Junction Temperature		+150	˚C	
Storage Temperature		-55~+150	˚C	

DC/AC Characteristics

Table 4

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Supply Voltages					
Pin VDD input		3.1		5.5	V
Chip Consumed Current	5.0V Supply Voltage Ta=25°C		2		mA
Error Amplifier Reference Voltage					
Non-Inverting input of the error amplifier	Measure INN VDD=3.1~5.5V, Ta=25°C	1.2125	1.25	1.2875	V
Line regulation			2	20	mV
Under Voltage Lock Out					
Positive Going Threshold	Ta=25°C Note3		2.7		V
Hysteresis		0.05	0.1	0.15	V
IC On/Off Control					
Turn On Threshold	Note3	1.5			V
Turn Off Threshold				0.3	V
High Frequency Ramp Wave Generator					
Operating Frequency	Note1	50		200	KHz
Output peak (CTOSC)			1.75		V
Output valley (CTOSC)			0.5		V
Accuracy	VDD=5V, Ta=25°C, 100KHz, 820pF Cap.	-3		+3	%
Error Amplifier					
Input voltage	Note2	0.1		3	V
Open loop gain		60	80		dB
Unit gain band width		1	1.5		MHz
Power On Initialization and Latched Off Protection Enable					
Pin TIMER Output current Case1. TIMER <0.3V	VDD=5.0V, Ta=25°C		20		uA
Pin TIMER Output current Case1. TIMER > 0.3V			1.0		uA
Power On Reset/Initialization threshold on pin TIMER			0.3		V
Latched Off Protection enable threshold on pin TIMER			1.8		V
SST Soft Start					
Output Current of SST			10		uA
SEN1 Detection					
Pin SEN1 fault detection lower threshold	VDD=5.0V, Ta=25°C	1.1	1.3	1.5	V
Hysteresis			20		mV
SEN2 Detection and Regulation					
Pin SEN2 detection lower threshold	VDD=5.0V, Ta=25°C	1.3	1.5	1.7	V
Hysteresis			20		mV
INN pin pull-up current source			60		uA
Operation Amplifier					
Non-inverting input voltage	VDD=5.0V, Ta=25°C		1.25		V
Max. output current				2	mA
Output					
CMOS output impedance	(Note2, Note3)		50		ohm
Rising Time	VDD=5.0V, 2000pF(Note2, Note3)		110		nS
Falling Time			100		nS
Delay Time			500		nS

Note 1. The frequency of OUT1, OUT2 is the half of the CTOSC frequency.
Note 2. Only guaranteed by design or sampled evaluation during 0 ~ 85°C. Not 100% tested.
Note 3. The OUT1 is pulled to GND in off state. The OUT2 is pulled to GND when MODE=0 and pulled to VDD when MODE=1 in off state.

Timing Diagram

BIT3501 uses fixed frequency driving methodology. The detail timing relationship is shown as bellow. The maximum duty cycle of OUT1 and OUT2 are always < 50% with 180° phase shift. The lower voltage (CMP or SST) determines the duty cycle of the output.

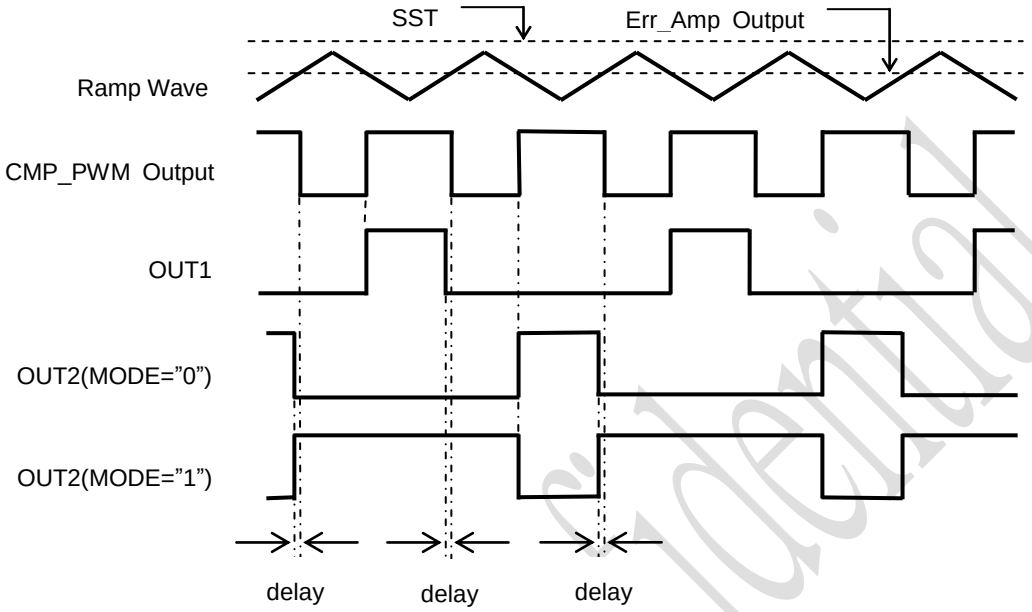


Fig.5

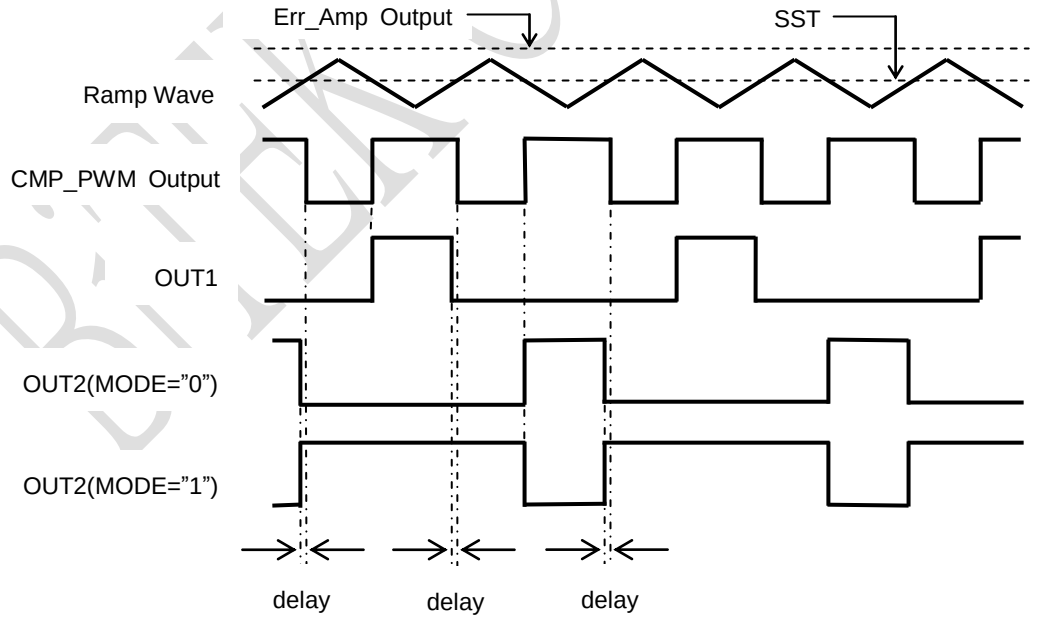


Fig.6

Layout Notice:

Some of the pins are very sensitive to noise. Please follow the bellowing guideline to make the layout:

Note 1. Please keep the capacitor between VDD and GND as close as possible. Noisy IC VDD may trigger UVLO or causes EOS (Electrical Over Stress). Fig. 7 is an example of making shortest traces between VDD and GND. The layout traces are under the IC.

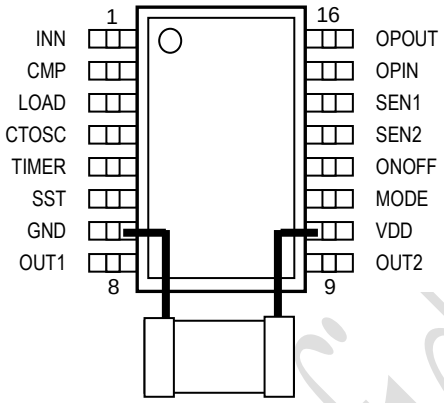
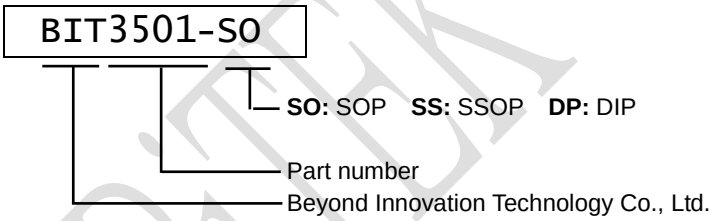


Fig. 7

Order Information:



P/N	Package	MOQ	SPQ	Remarks
BIT3501-SO	SOP16	2500	2500 / Reel	Green
BIT3501-SS	SSOP16	2500	2500 / Reel	Green

Soldering Information:

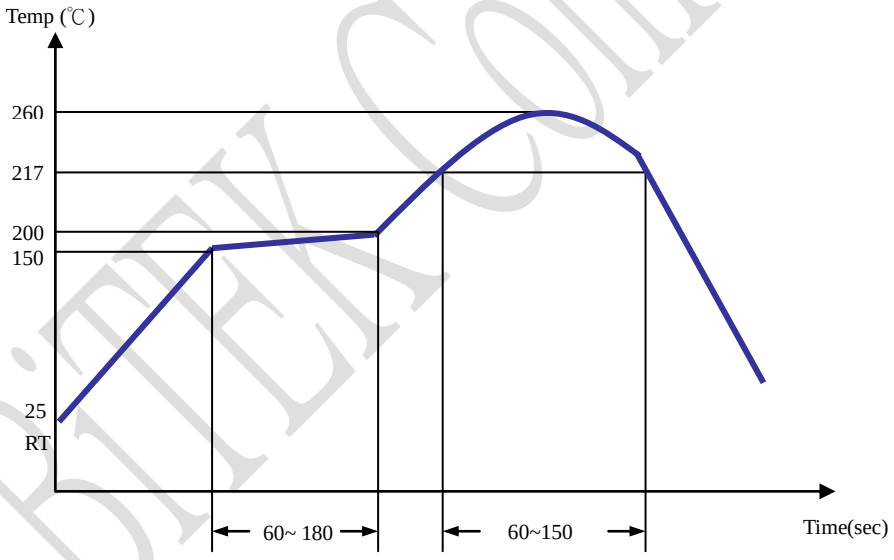
Reflow Soldering:

The choice of heating method may be influenced by plastic QFP package). If infrared or vapor phase heating is used and the package is not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stenciling or pressure-syringe dispensing before package placement. Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferable be kept below 245 °C for thick/large packages (packages with a thickness ≧ 2.5 mm or with a volume ≧ 350 mm^3 so called thick/large packages). The top-surface temperature of the packages should preferable be kept below 260 °C for thin/small packages (packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called thin/small packages).

Stage	Condition	Duration
1'st Ram Up Rate	max3.0+/-2℃/sec	-
Preheat	150℃~200℃	60~180 sec
2'nd Ram Up	max3.0+/-2℃/sec	-
Solder Joint	217℃ above	60~150 sec
Peak Temp	260 +0/-5℃	20~40 sec
Ram Down rate	6℃/sec max	-



Wave Soldering:

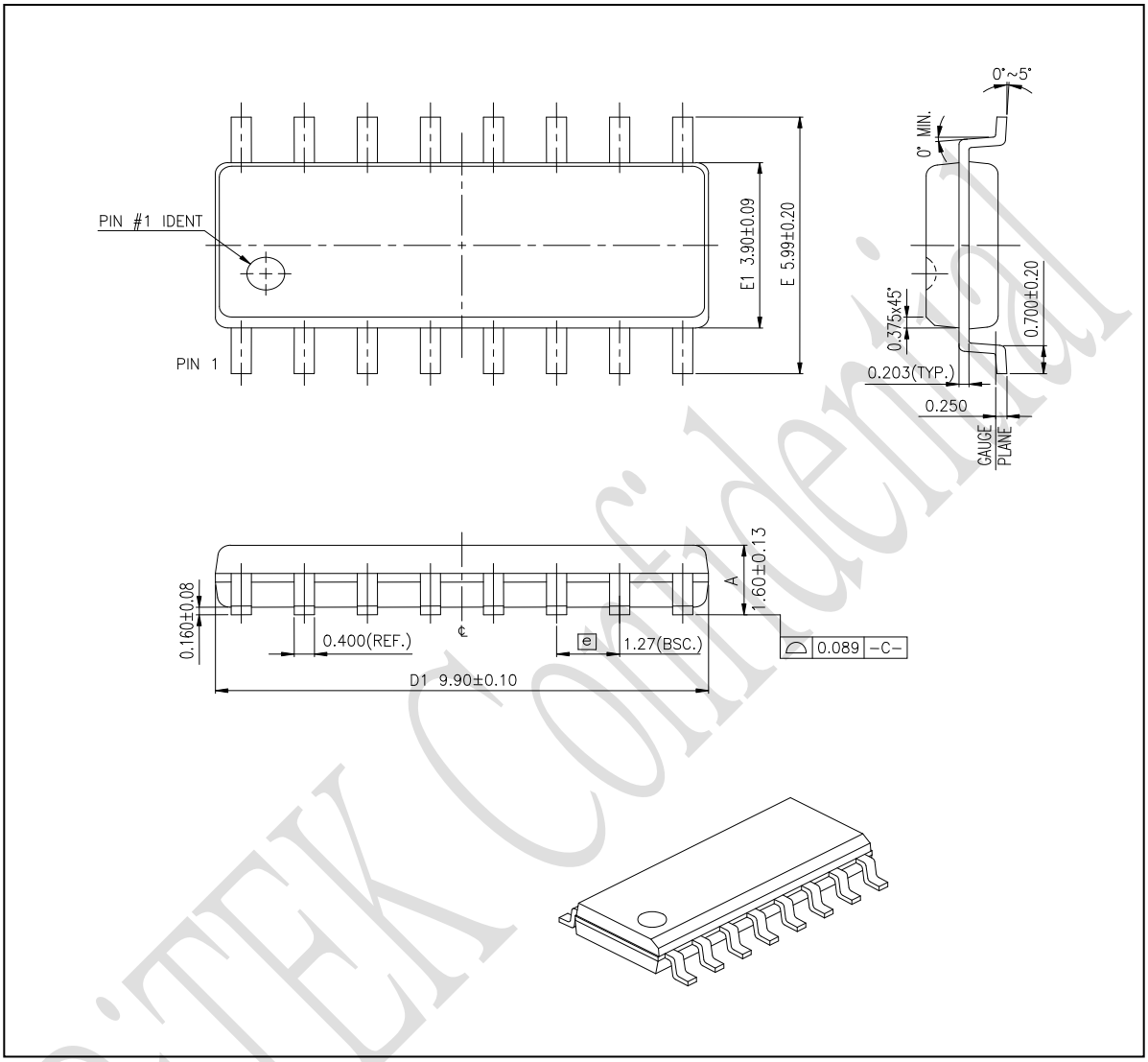
Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

Manual Soldering:

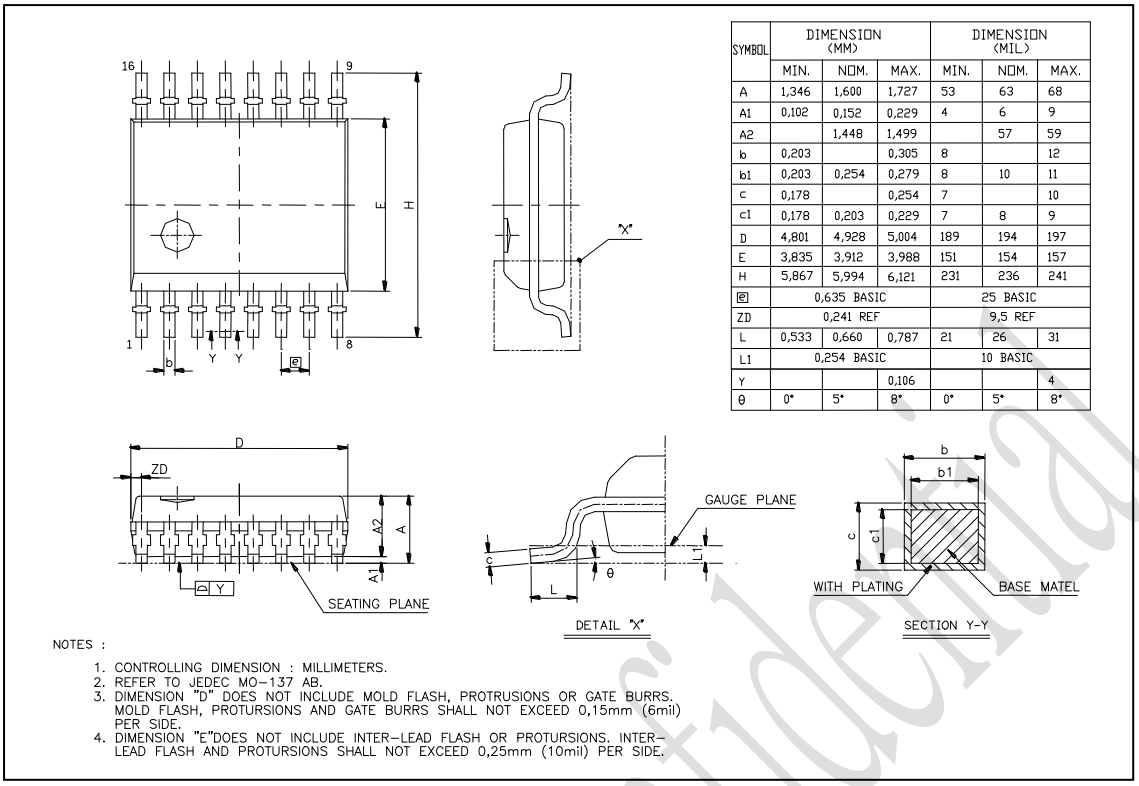
Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Package Information:

SOP type:



SSOP type:

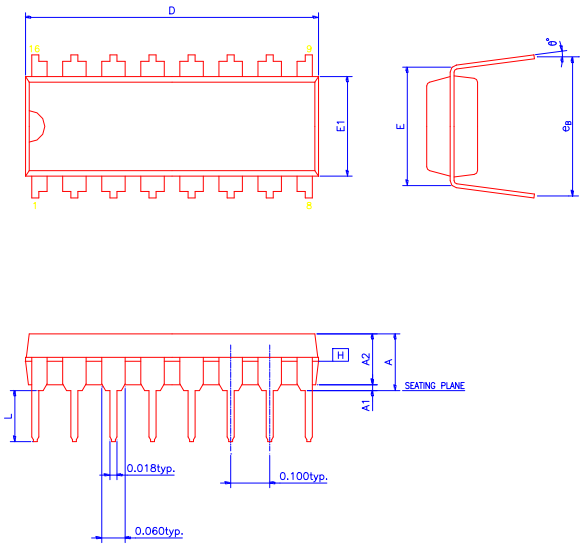


SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1,346	1,600	1,727	53	63	68
A1	0,102	0,152	0,229	4	6	9
A2		1,448	1,499		57	59
b	0,203		0,305	8		12
b1	0,203	0,254	0,279	8	10	11
c	0,178		0,254	7		10
c1	0,178	0,203	0,229	7	8	9
D	4,801	4,928	5,004	189	194	197
E	3,835	3,912	3,988	151	154	157
H	5,867	5,994	6,121	231	236	241
e	0,635 BASIC			25 BASIC		
ZD	0,241 REF			9,5 REF		
L	0,533	0,660	0,787	21	26	31
L1	0,254 BASIC			10 BASIC		
Y			0,106			4
θ	0°	5°	8°	0°	5°	8°

NOTES :

1. CONTROLLING DIMENSION : MILLIMETERS.
2. REFER TO JEDEC MO-137 AB.
3. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTURSIONS AND GATE BURRS SHALL NOT EXCEED 0,15mm (6mil) PER SIDE.
4. DIMENSION "E"DOES NOT INCLUDE INTER-LEAD FLASH OR PROTURSIONS. INTER-LEAD FLASH AND PROTURSIONS SHALL NOT EXCEED 0,25mm (10mil) PER SIDE.

DIP type:



SYMBOLS	MIN.	NOR.	MAX.
A	–	–	0.210
A1	0.015	–	–
A2	0.125	0.130	0.135
D	0.735	0.755	0.775
E		0.300 BSC.	
E1	0.245	0.250	0.255
L	0.115	0.130	0.150
e_B	0.335	0.355	0.375
θ°	0	7	15

UNIT : INCH

NOTES:

1. JEDEC OUTLINE : MS-001 BB
2. "D","E1" DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH.
3. eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
4. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
5. DISTANCE BETWEEN LEADS INCLUDING DAM BAR PROTRUSIONS TO BE .005 INCH MININUM.
6. DATUM PLANE [H] COINCIDENT WITH THE BOTTOM OF LEAD, WHERE LEAD EXITS BODY.